Integrating the S800 with other systems

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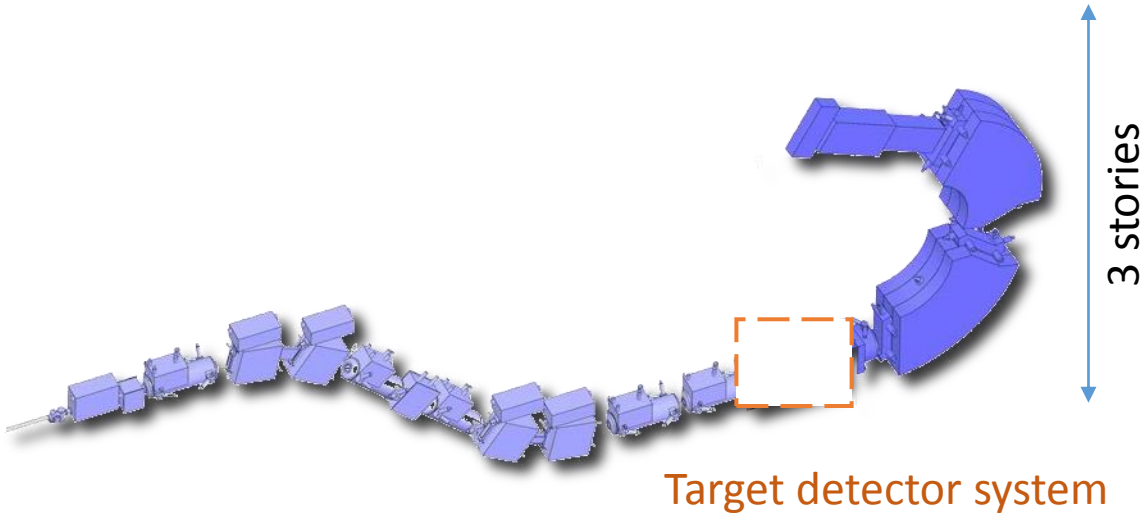
NSCL

Overview

- Overview of DAQ systems involved
- Common Challenges
- Issues with timestamping
- Debugging
- Summary

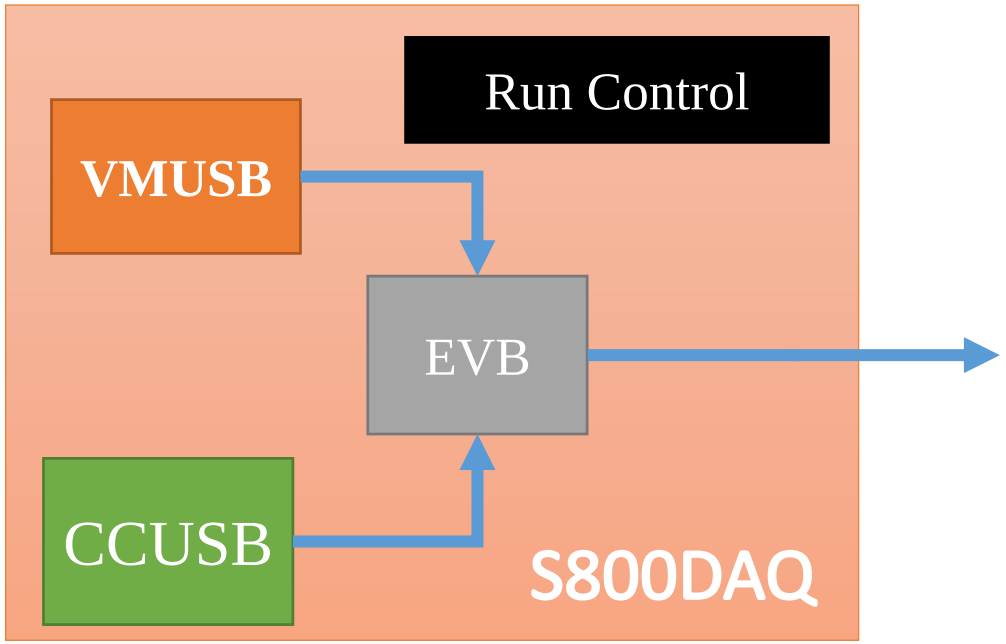
The S800 Spectrograph

- Analysis Line PPACS
- Focal plane detector box:
  - Ion chamber (32 channels)
  - CRDCs (224 channel per CRDC)
  - Hodoscope CsI array (32 channels)
  - Fast scintillator (1 channel)
- Target position detector



The S800 DAQ

- ULM trigger logic module (fw: Daniel Bazin)
  - Accepts triggers for S800 + 3 other trigger sources
  - Internal busy OR
- Clock generator or receiver
- Master/slave run control modes
- Not NSCLDAQ software
- “Traditional” front-end electronics



Target DAQ

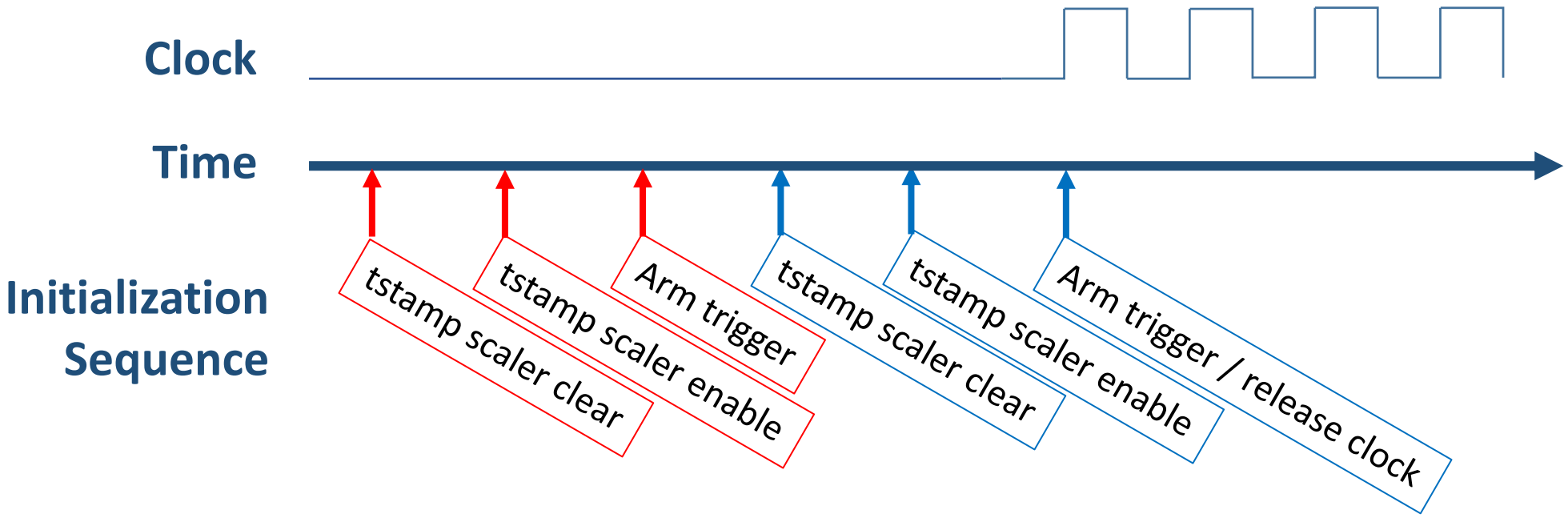
	VMUSB	DDAS
Style	Traditional	Digital
Hardware/Software interface	VMUSBReadout	DDASReadout
Timestamp mechanism	Latching scaler	Internal
Trigger	External NIM	External NIM / Internal
Busy	VMUSB produced	“None”
Hardware compatibility	Any VME device	XIA digitizers

Challenges to Unifying S800 + Target DAQ

- Establishing repeatable timestamp synchronization
- Trigger configuration
- Who generates the clock signal?
- Clock frequency
- Data format differences
- Debugging with system interdependence
- Global run control

“Vetoed Clock” Synchronization

- Controlled initialization order
- Clock only outputted when DAQ active



Issues with “Vetoed Clock” Synchronization

- At least one of the systems must be able to:
  - output an ON/OFF level to veto the clock
  - receive an external clock
- No standard means to do it

BETTER Solution:

- All systems required to receive external clock
- All systems required to receive external clear
- Provide external clock generator that can provide a hardware clear

Frequency Discrepancies

System/Device	Max Input Frequency (MHz)	Output Frequency (MHz)
S800 ULM Trigger	40	10
S800 VME Timestamp Module	80	-
VMUSB	< 100 MHz	80
DDAS	?	50

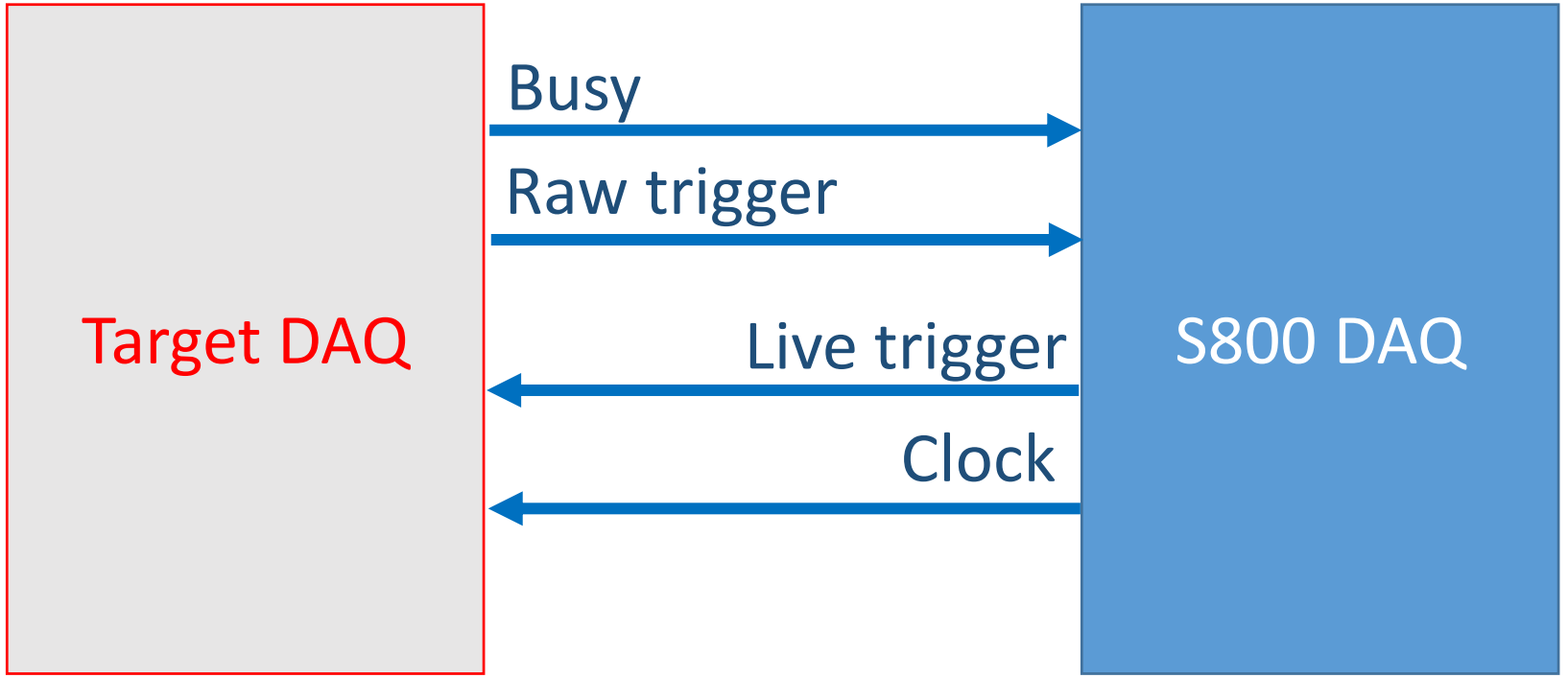
Example: DDAS + S800 ; DDAS as clock generator:

- DDAS Output 50 MHz → Downscale x4 → 12.5 MHz to S800
- Meanwhile DDAS timestamps with its internal 100 MHz clock

Solution: user-defined timestamp calculation

Debugging the Unified System

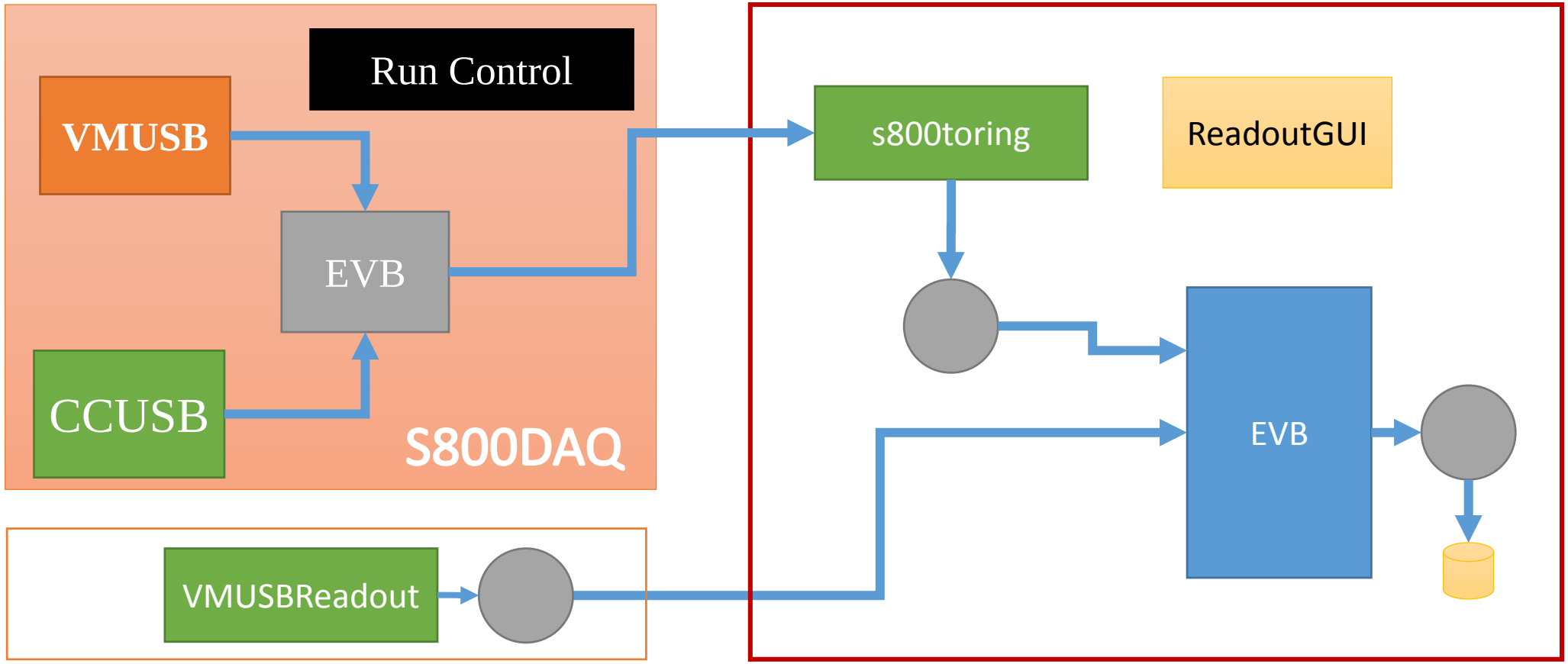
- How to isolate systems?
- Trigger?
- Busy?



Summary

- Unification is the norm and is nontrivial
- Clock synchronization is a custom job every time... hope for standardized approach
- Hardware is more commonly the difficult aspect, software already pretty flexible
- How do we improve debugging?

S800 + VMUSB Data Flow



S800 + DDAS Data Flow