High Performance Data Acquisition System For Underground Dark Matter Searches

Wojtek Skulski[1,2,3], David Hunter[1,3], Eryk Druszkiewicz[2,4], Dev Khaitan[2,4], Jun Yin[2,4], Frank Wolfs[2,4]

1) SkuTek Instrumentation http://www.skutek.com

2) Department of Physics and Astronomy, University of Rochester, http://teacher.pas.rochester.edu/

3) Supported by the Department of Energy, Phase II SBIR grant DE-SC0009543 *Low Cost, High-Density Digital Electronics for Experimental Physics*.

4) Supported by the Department of Energy, grant DE-SC0006605.

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LUX-ZEPLIN Collaboration

32 institutions

University of Alabama
SUNY, Albany
Lawrence Berkeley Laboratory (LBNL)
Brookhaven National Laboratory (BNL)
Brown University
University of California, Berkeley
University of California, Davis
University of California, Santa Barbara
Daresbury Laboratory (UK)
Edinburgh University (UK)
Fermi National Laboratory
Imperial College London (UK)
Lawrence Livermore National Laboratory
LIP Coimbra (Portugal)
University of Liverpool (UK)
University of Maryland
University of Michigan
MEPhI (Russia)
Northwestern University
University of Oxford (UK)
University of Rochester
Rutherford Appleton Laboratory (UK)
University of Sheffield (UK)
University of South Dakota
SLAC National Accelerator Laboratory
South Dakota School of Mines & Technology
South Dakota Science & Technology Authority
Texas A&M University
University College London (UK)
Washington University
University of Wisconsin
Yale University

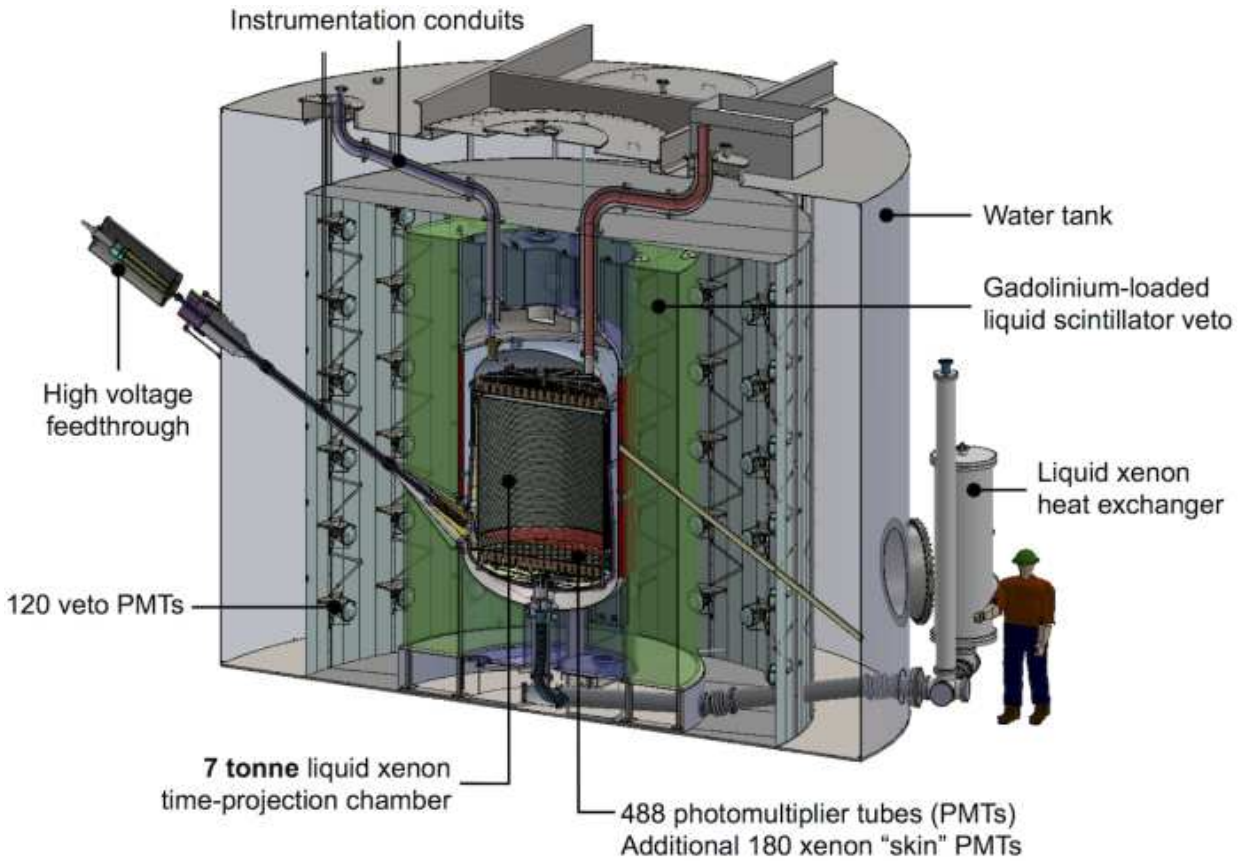
LZ is a continuation and expansion of that is installed in the Davis Cavern @ SURF.

LZ will be 20 times larger than LUX

LZ will be installed in the same water tank that is now occupied by LUX.

- Amount of Xenon:
  - 5.6 tons fiducial
  - 7 tons in the vessel
  - 10 tons total.
  - Drift time in Xenon: 700 μs.
- Number of PMTs:
  - 488 main volume (dual gain)
  - 180 “skin”
  - 120 veto
  - Total **788** PMTs.
- Electronic channels:

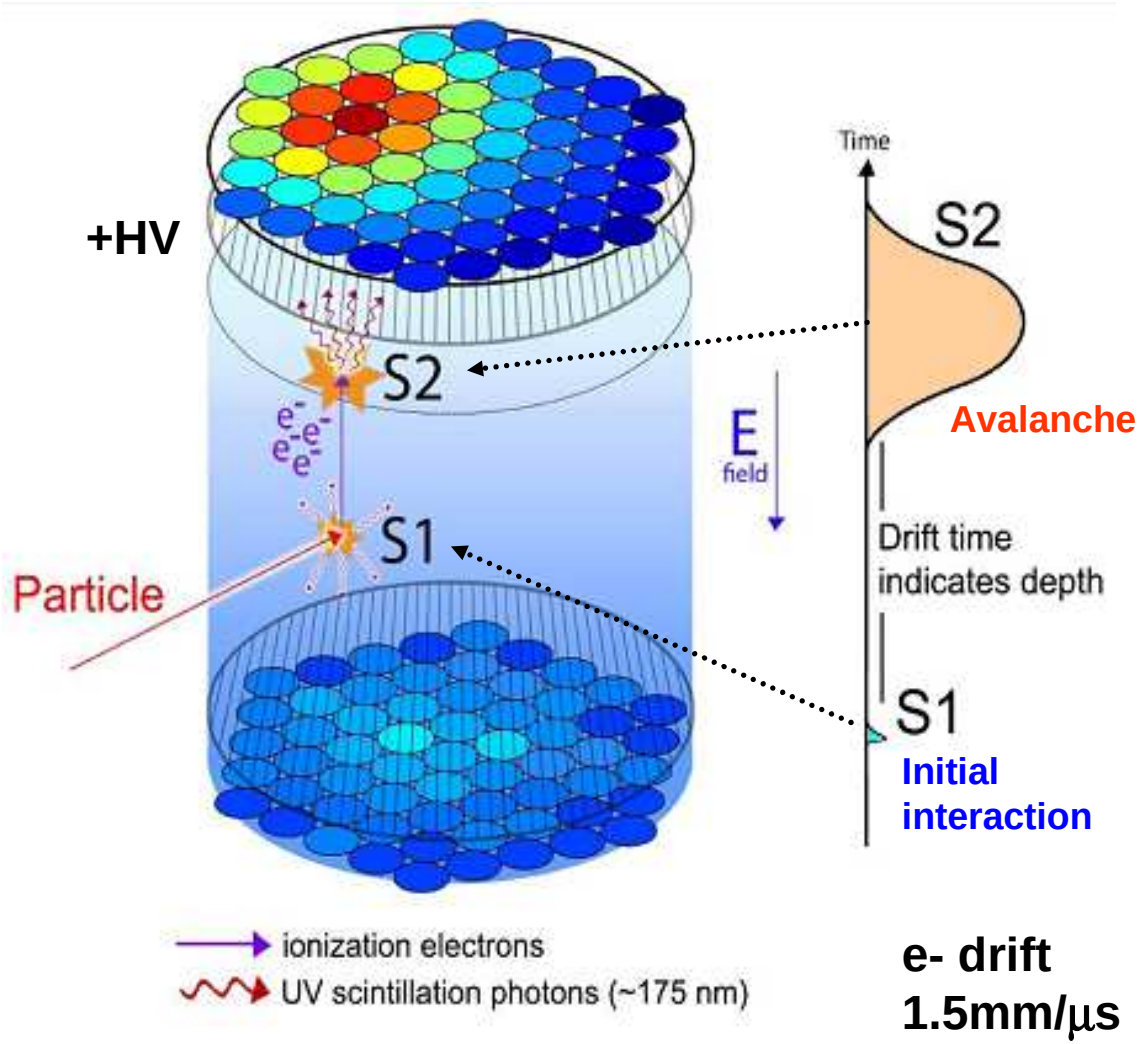
  2*488 + 180 + 120 = **1,276**.



Event processing in LZ is based on the concept of “data sparsification” = real time data selection utilizing the results of waveform analyses of individual S1 and S2 signals.

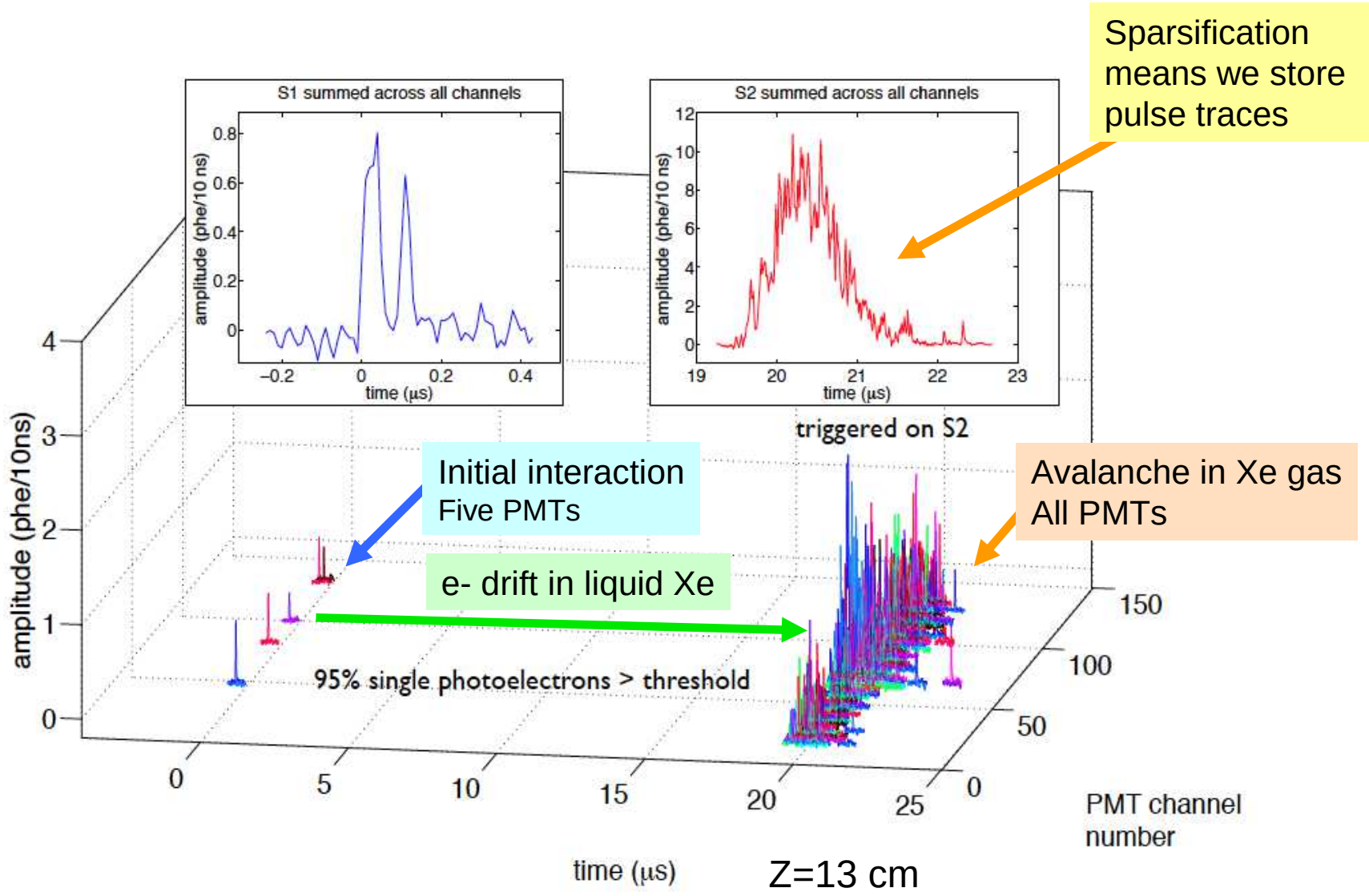
Two-Phase Xenon TPC for Dark Matter Search

- **S1: LXe is an excellent scintillator**
  - Density: 3 g/cm^3
  - Light yield: ~70 ph/keV (0 field)
  - Scintillation light: 178 nm (VUV)
  - **Nuclear recoil threshold ~5-10 keV**
- **S2: Even better ionisation detector**
  - Sensitive to single ionisation electrons
  - **Nuclear recoil threshold ~1 keV**



Tim Sumner, APC, Paris 12/17/2013

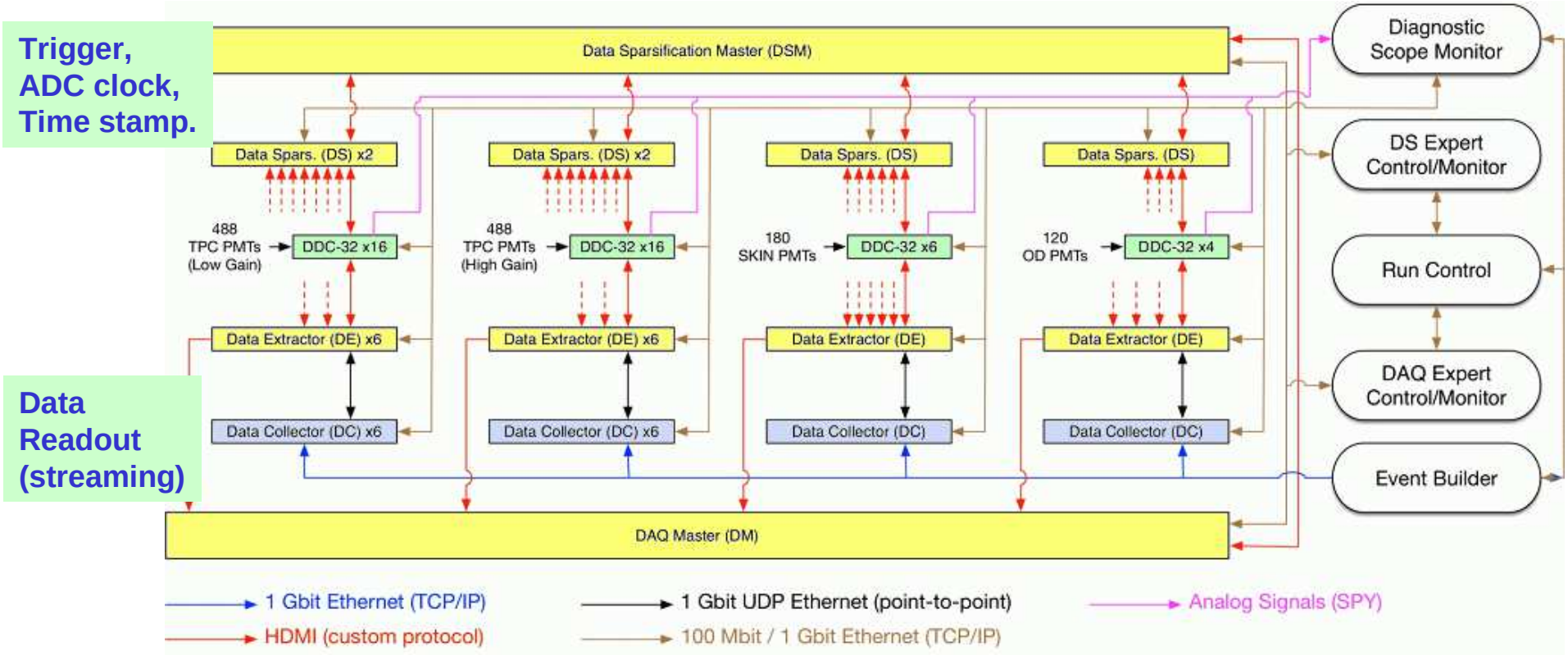
LUX event with 1.5 keV electron recoil



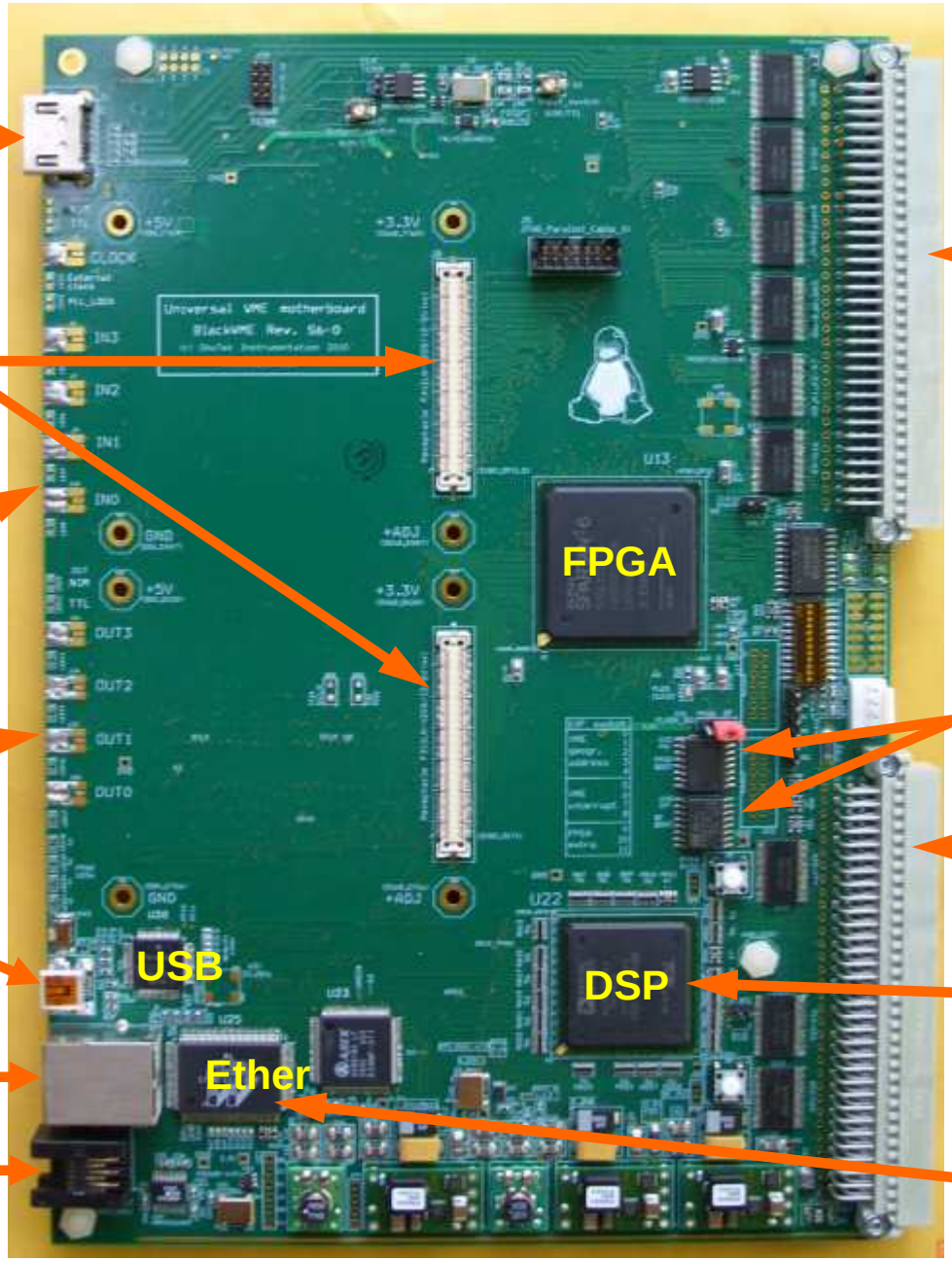
Frank Wolfs, UofR Colloquium, Rochester 12/04/2013

DAQ Architecture with Digitizers, Logic Units, and Collectors.

- The DAQ is being developed by University of Rochester in close collaboration with SkuTek.
  - **42 digitizers**: 32 channels, 14 bits @ 100 MSPS, low noise (~1.3 LSB).
  - **22 logic units**: event preprocessing and real time sparsification. Also ADC clock and time stamp.
  - **14 data collectors**: off-the-shelf PC units and disk arrays.
  - Total data rate that the DAQ can potentially handle: 14 collectors * ~100 MB/s each = 1,400 MB/s.
  - Cost effective thanks to high channel density (32 ADC's per digitizer).
  - Trigger and the DAQ integrated using fast point-to-point SerDes links.



The Foundation: Digital Motherboard with VME-64, SerDes, and Linux



Point-to-point link
LVDS SerDes
Data, clock,
time stamp

Two daughter
connectors,
110 I/O's each

4*logic IN
NIM or TTL

4*logic OUT
NIM or TTL

USB-2

Ethernet from DSP

RS-232

VME P1

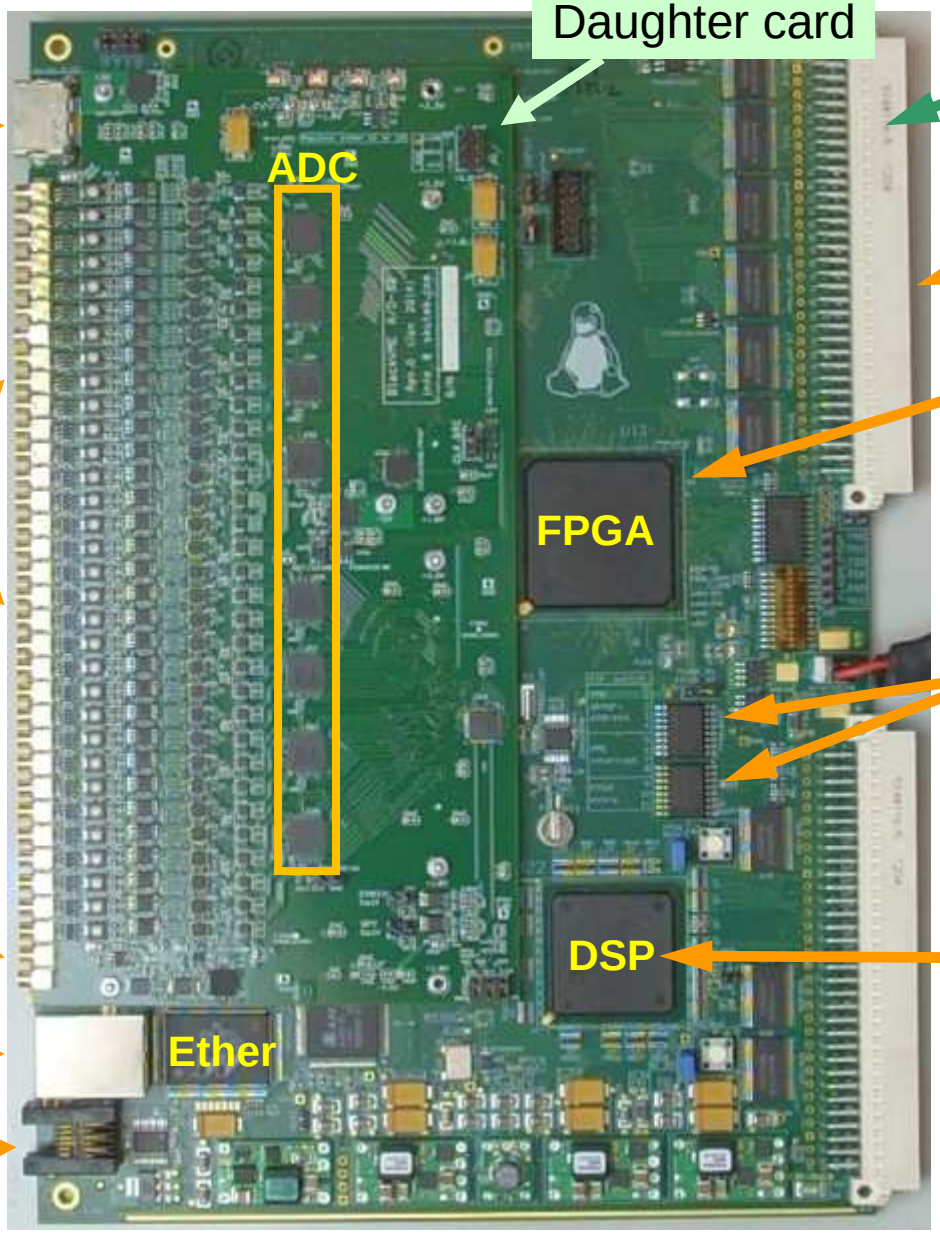
Flash chips:
Linux system
and FPGA
firmware

VME P2

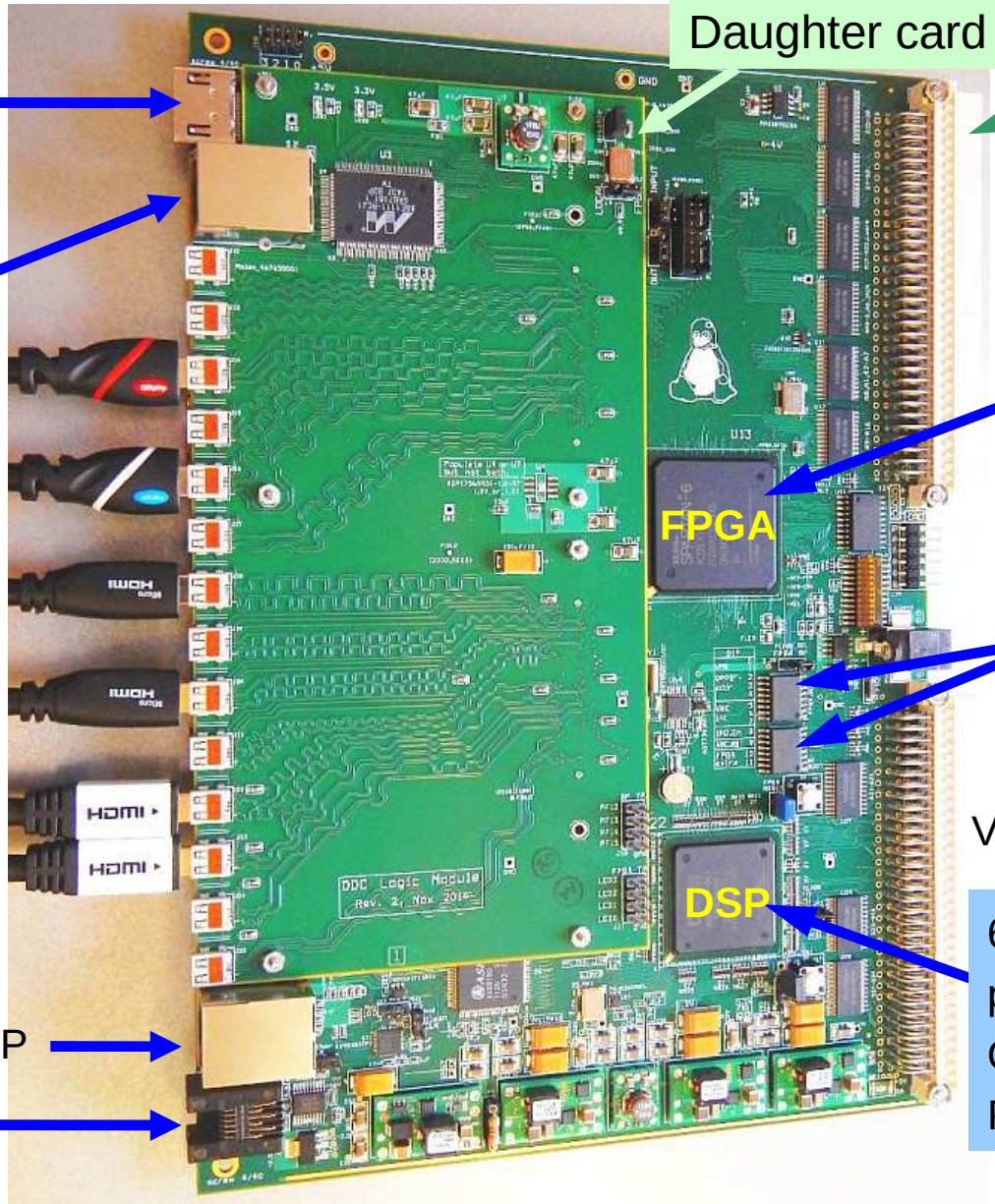
600 MHz dual core
ONLINE
PROCESSING

PTP time stamping
hardware is included

Digitizer DDC-32 = 32-channels, 14 bits, 100 MSPS



Logic Unit: Trigger, Data Readout, ADC Clock, Time Stamp.



The Digitizer Connection with the Logic Unit

Up to 14
SerDes links:
Data, clock, TS

Data, ADC clock, TS

Each link:
1.8 Gbit/s
225 MB/s
as of Jul/24/2015

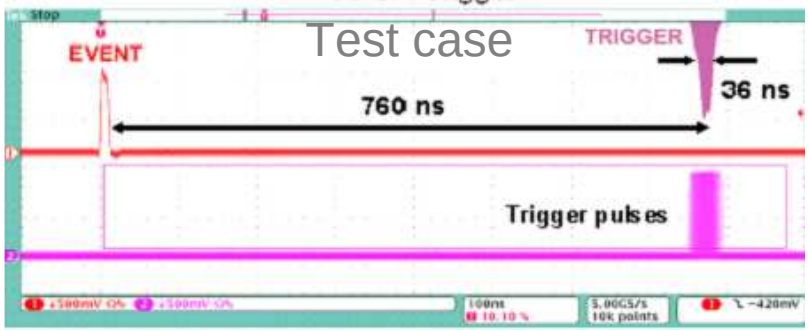
The LVDS Links use
standard HDMI cables

225 MB/s to the next Logic level

Full GbE speed to Data Recorder

Ethernet for control and monitoring

FPGA Trigger
Test case



LZ - Data Collector

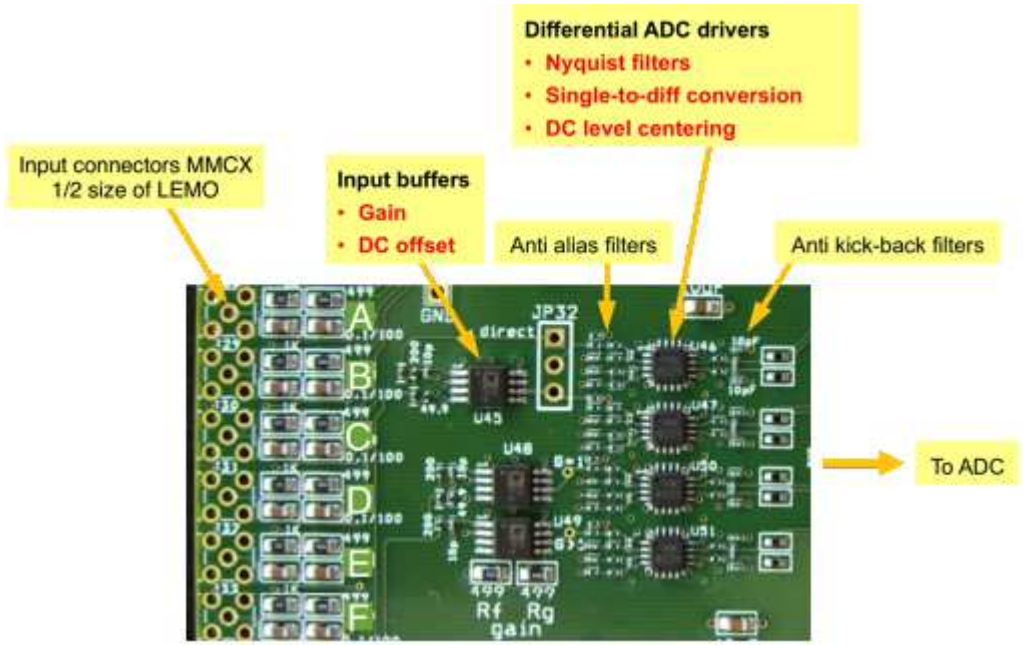
Work by Eryk Druszkiewicz

Components of the tested Data Collector prototype:

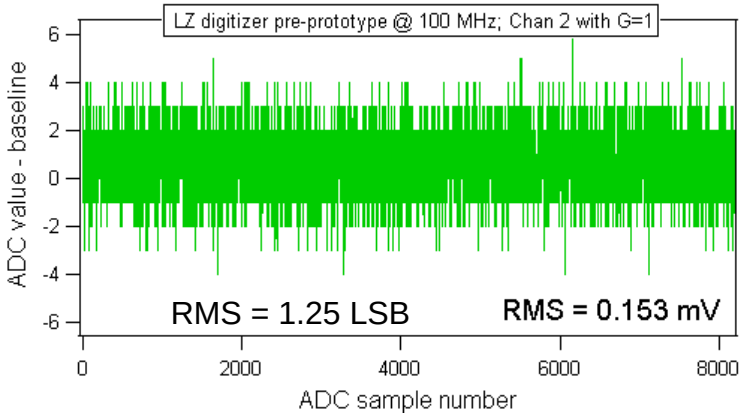
Processor:	Intel Xeon E3-1270V3 3.5GHz Quad-Core	**HDD:**	SAMSUNG 840 Pro Series 256GB SSD
Motherboard:	ASUS P9D-V ATX		Western Digital RE4 4TB 7200 RPM
Memory:	16GB Kingston DDR3 SDRAM ECC	**Case:**	NORCO RPC-270 2U Server Case
NIC:	Intel Ethernet Server Adapter I350-T2	**Hot Swap:**	ICY DOCK 3.5" and 2.5" SATAIII HDD Rack Tray

Off-the-shelf system components

Performance of the Prototype ADC Channel

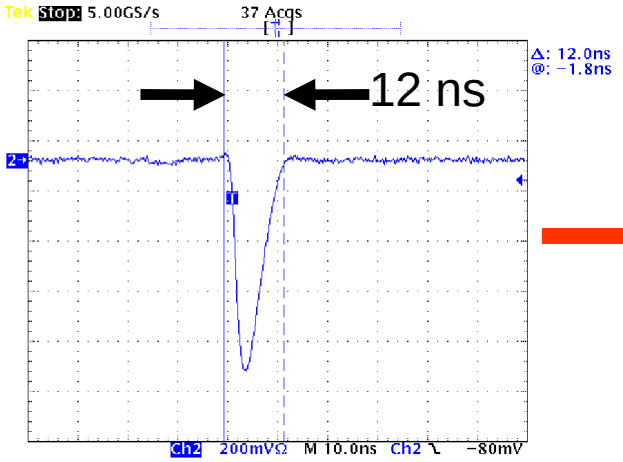


Free run noise waveform.
Digitizer input terminated with 50 ohms.

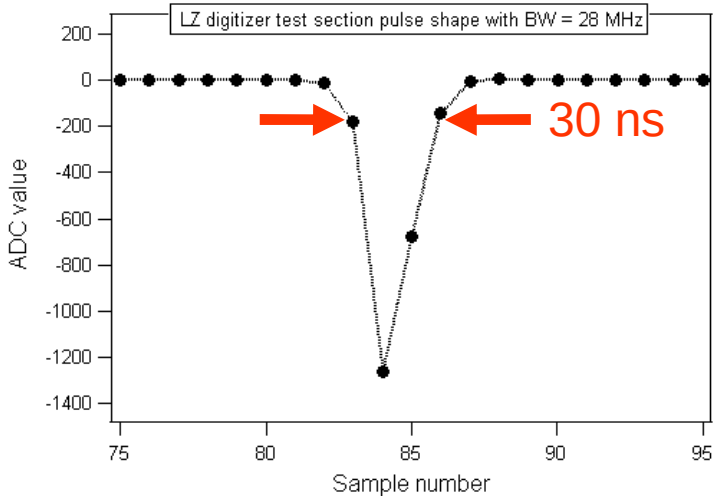


The on-board anti-alias filter is shaping the input pulses to ensure that even the fastest pulses are digitized with an adequate number of samples.

Similar to PMT pulse



Response to a 12 ns pulse*
*Total width



Ways to integrate this electronics with FRIB

1. Each motherboard is equipped with a standard VME-64 interface
   - We developed the VME readout with a Wiener VM-USB using the Wiener GUI.
   - We provide a C driver library to use any VME controller.
   - Integration with the MSU NSCL infrastructure should be easy.
2. Each motherboard is running Linux which can be networked for readout, monitoring, and control.
   - Limited form of online analysis directly on board close to the signals.
   - The embedded Linux is optional. If it is not needed then it can be turned off. (The straightforward VME readout does not need the on-board Linux.)
3. Each motherboard has a front-panel HDMI connector for SerDes link to the Logic Module.
   - Logic Module can serve as the **Trigger Module** for up to 14 digitizers.
   - Logic module can serve as the **Data Streaming Module** (full GbE speed to the Data Recorder).
   - Both approaches will be used for LZ.
4. ADC clock and time stamps are distributed throughout the entire system using the LVDS links.
   - Clocking signals can be either sent or received because the links are bidirectional.
5. Every motherboard has front panel NIM inputs and outputs.
   - The FPGA firmware can accommodate external NIM trigger and/or veto.

Status and plans

- The LZ DAQ with **1,276** readout channels is under development. A small scale prototype system will be tested this Fall. (Two Digitizers, three Logic Modules.)
- We will incorporate lessons from the test system into our final design.
- The following DAQ modules are available **now**:
  - **Digitizer**: **32** channels, 14 bits @ 100 MSPS, low noise (available now).
  - **Logic Unit**: 14 LVDS sockets, event preprocessing, triggering, and data streaming (now).
- VME compatible modules are available now or will be available this year.
  - **Digitizer**: **10** channels, 14 bits @ 100 MSPS (now).
  - **Digitizer**: **10** channels, 14 bits @ 250 MSPS (early Fall).
  - **Digitizer**: **40** channels, 14 bits @ 100 MSPS (late Fall).
- FemtoDAQ modules are available this Fall.
  - **FemtoDigitizer**: **2** channels, 14 bits @ 100 MSPS, very low cost **<$1k** (now).
  - **SiPM Bias Module**: part of the FemtoDAQ System, one output 10V to 90V (now).
- Linux System On Module (SOM) with real time coprocessors: Winter or early Spring
- Additional electronic modules, firmware, and R&D, as requested by the community.

Please tell us what you need!

Our work is funded by the DOE Office of Science to help the research community. We would like to hear from you what are your needs for electronic measurement equipment.

- We can develop:
  - Digitizers,
  - Logic and Trigger modules,
  - QDCs, TDCs,
  - and other electronics needed by the community.
- We can commercialize electronics developed by the research groups.
- We can pursue SBIR funding to help you advance FRIB projects.
- Please tell us what you need.
- We will work together with the FRIB community to develop solutions that you need.

LZ DAQ Summary

- LUX-Zepplin (LZ) is the next generation LXe Dark Matter detector with 5.6 tons active volume.
- The detector will be equipped with 788 PMTs and **1,276** readout channels.
- A sophisticated, self-triggered DAQ is under development in Rochester:
  - **42 digitizers**: 32 channels, 14 bits @ 100 MSPS, low noise (~1.3 LSB).
  - **22 logic units**: event preprocessing and real time sparsification.
  - **14 data collectors**: off-the-shelf PC units and disk arrays.
- The DAQ electronics is now tested at the Dept. of Physics & Astronomy, Univ. of Rochester.
  - Digitizer RMS noise ~1.3 ADC counts (about 160 μV).
  - Data transfer from the Digitizer FPGA to the Logic FPGA at 225 MB/s.
  - Data transfer from the Logic FPGA to the Collector at full GbE speed.
  - Pulse detection algorithms are well developed as a result of LUX Trigger project.
- Run Control software is under development at Washington Univ. @ St. Louis.
- Analog electronics front end is under development at UC Davis.
- A small System Test will consist of two digitizers and three Logic modules. The measurements will be conducted this Summer/Fall.
- The lessons from the test system will be incorporated into the final design.