



Data Acquisition for Collinear Laser Spectroscopy

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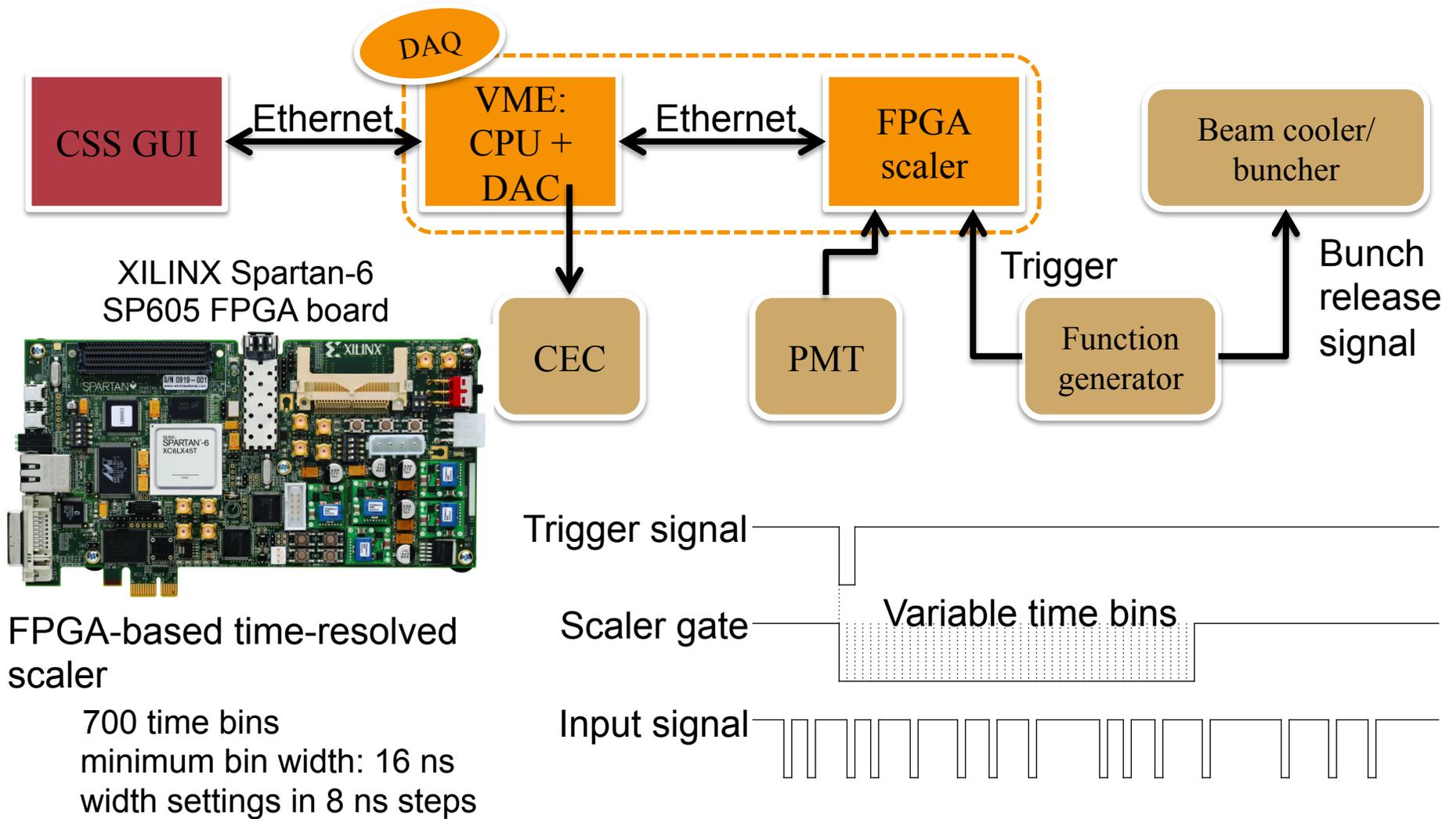


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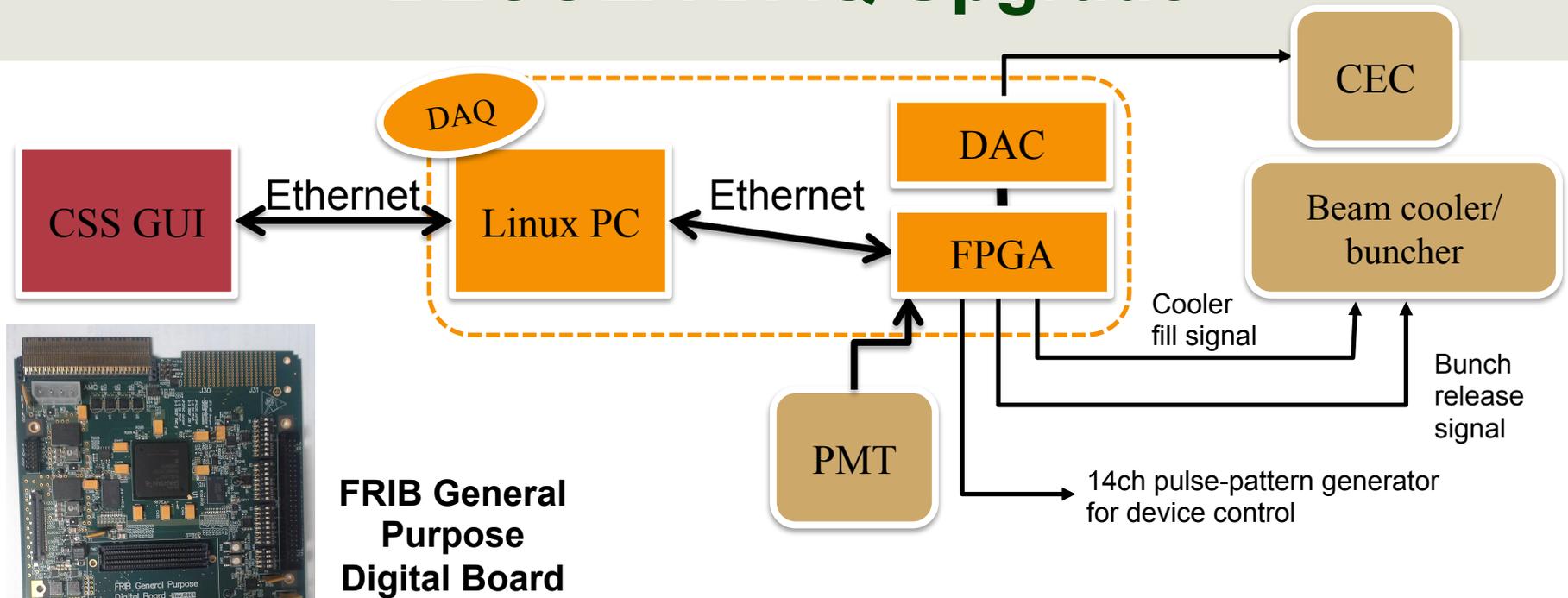
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BECOLA DAQ Initial Implementation



BECOLA DAQ Upgrade



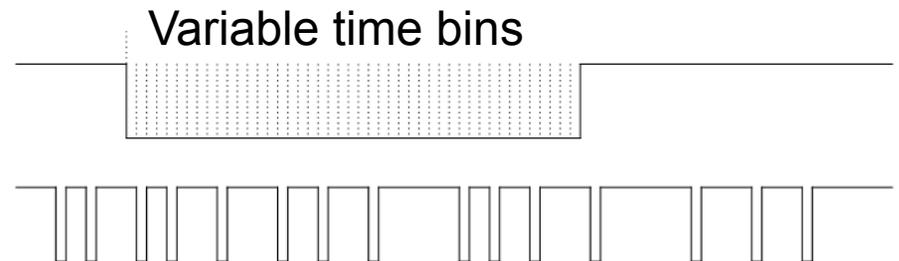
FRIB General Purpose Digital Board

FPGA-based time-resolved scaler

1024 time bins (max)
 minimum bin width: 16 ns
 width settings in 8 ns steps

Scaler gate

Input signal



Variable time bins

BECOLA DAQ

Where are we going?

- **Eliminate need for intermediate PC**
 - Introduce CPU into FPGA housing (local processing)
- **Data packets**
 - UDP protocol
 - Sequence-driven organization of data packets by driver
 - Transmitted across network
- **Continue with CS-Studio GUI interface**
 - Lab “standard”
 - Advantage of platform-independent operation
 - Access to parameters for DAC, Scaler, and data packets
- **Analysis**
 - On-line
 - » Data stream “picked up” by CS-Studio
 - » Histogramming using standard packages in CS-Studio
 - » Displayed via GUI
 - Off-line
 - » Data packets written to disk as binary files
 - » Converted to text files (e.g., Mathematica)
 - » Converted to ROOT files



BECOLA DAQ Performance

- **Data Transfer Rates**
 - 1 Gigabit Ethernet communication between FPGA and PC
- **Scaler Accumulation Rates**
 - Up to 100 MHz
- **Gating Limitations**
 - Up to 1024 identical scaler bins, or up to 64 configurable (non-identical) scaler bins
 - 16 ns minimum gate width, adjustable in 8 ns steps
- **Dead Time**
 - Dwell time as low as 16 ns (depends on gate settings)
- **FPGA functionality**
 - Lab “standard”
 - 16 fast inputs
 - 16 outputs (14 configurable pulse-pattern generator)
- **DAC functionality**
 - 1 output
 - 20 bits

