High Performance Digital Electronics with Embedded ARM and Linux*)

Wojtek Skulski

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SkuTek Instrumentation

SkuTek.com

UNIVERSITY of ROCHESTER

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Outline

- The DAQ challenge: LUX-Zepplin detector with 1,359 channels.
- Custom data acquisition electronics for LUX-Zepplin.
- The benefit of upgrading the electronics using the ARM processor and Kintex-7.
- A broader landscape: the **Cloud** versus the **Fog**.
- The benefits of the Fog.
- FemtoDAQ can become the test bed for the Fog development.

LUX-Zepplin detector will use our DAQ electronics

SkuTek collaboration with UofR Physics and Astronomy

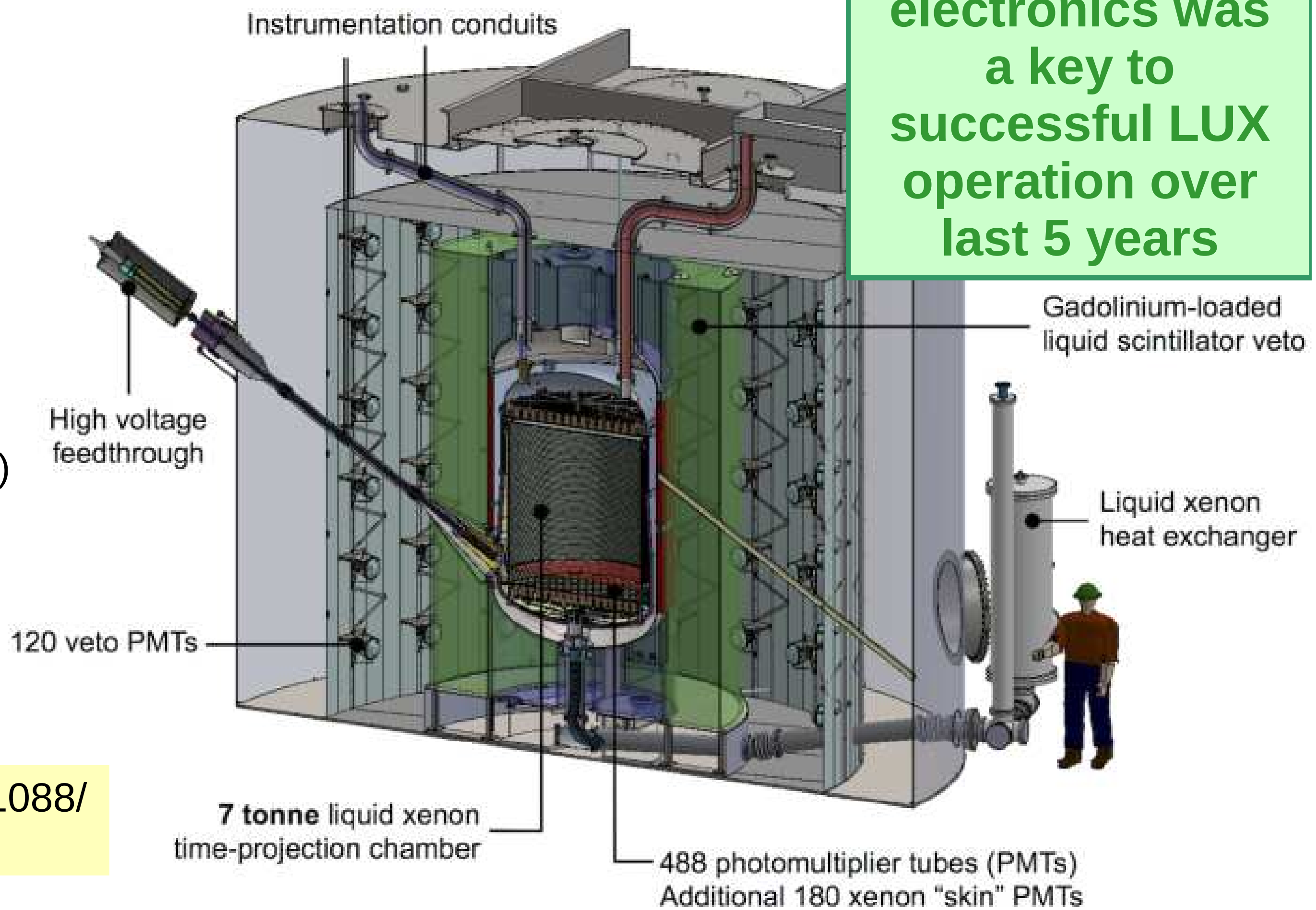
UNIVERSITY of ROCHESTER

LUX-Zepplin is the "ultimate Dark Matter Search Detector" under development by 32 institutions. We are building the digital DAQ for LZ with **1,359** channels.

SkuTek Digital Trigger electronics was a key to successful LUX operation over last 5 years

- Amount of Xenon:
  - 5.6 tons fiducial
  - 7 tons in the vessel
  - 10 tons total.
  - Drift time in Xenon: 700 μs.
- Number of PMTs:
  - 494 main volume (dual gain)
  - 131 "skin"
  - 120 outer detector veto (dual gain)
  - Total **745** PMTs.
- Electronic channels:

  2*494 + 131 + 2*120 = **1,359**.



http://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02072

LUX-Zepplin Data Acquisiton System

Custom VME modules: (1) a high density digitizer with 32 channels, and (2) a Trigger / Logic module with fast LVDS links. The prototypes use Blackfin processors and Spartan-6 FPGAs. The ARM + Kintex units are under development.

High density digitizer: 32 channels

32 channels

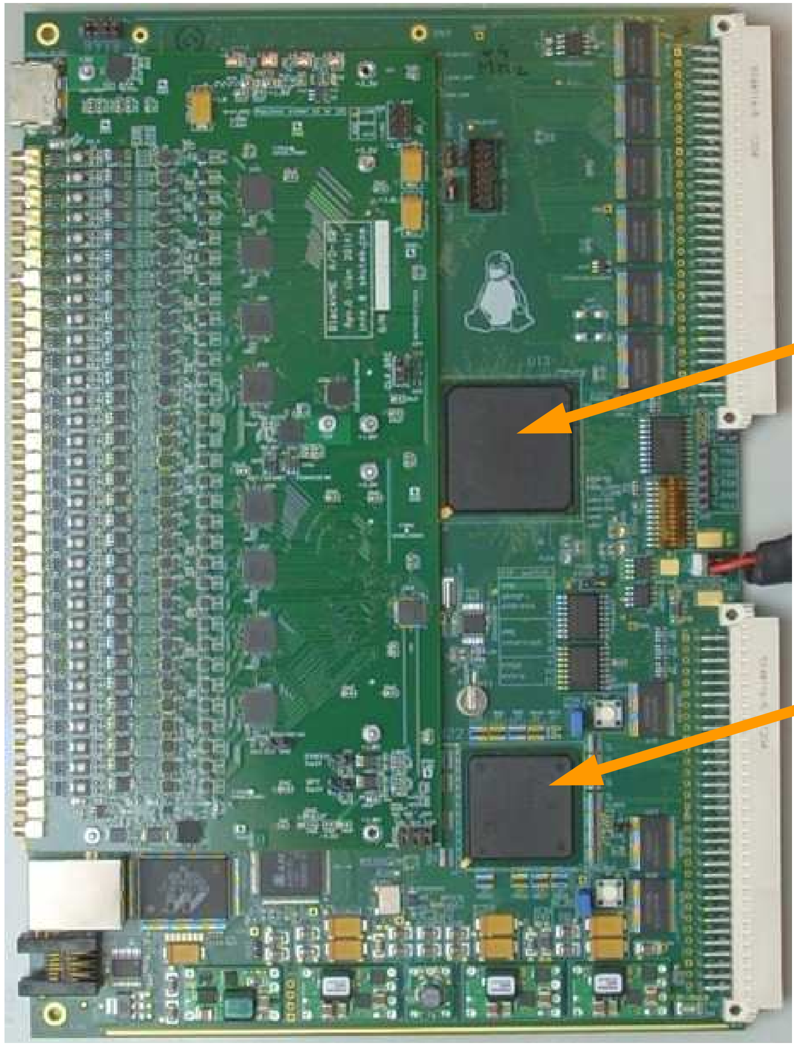
Trigger / Logic module

14 inputs

Upgrading the CPU and the FPGA

Upgrading the FPGA to Kintex-7 and the CPU to ARM will improve both the performance and the number of channels per board.

32 channels



FPGA upgrade
Spartan-6 to Kintex-7

CPU upgrade
Blackfin to ARM

MicroBone: Linux System on Module (SOM) with ARM, 2” by 3”

In order to upgrade our electronics, we developed the ARM Linux System on Module (SOM) with a low-power, high-performance 1 GHz ARM processor.

We will use it in our forthcoming electronics. The SOM module itself will also be offered to the community.

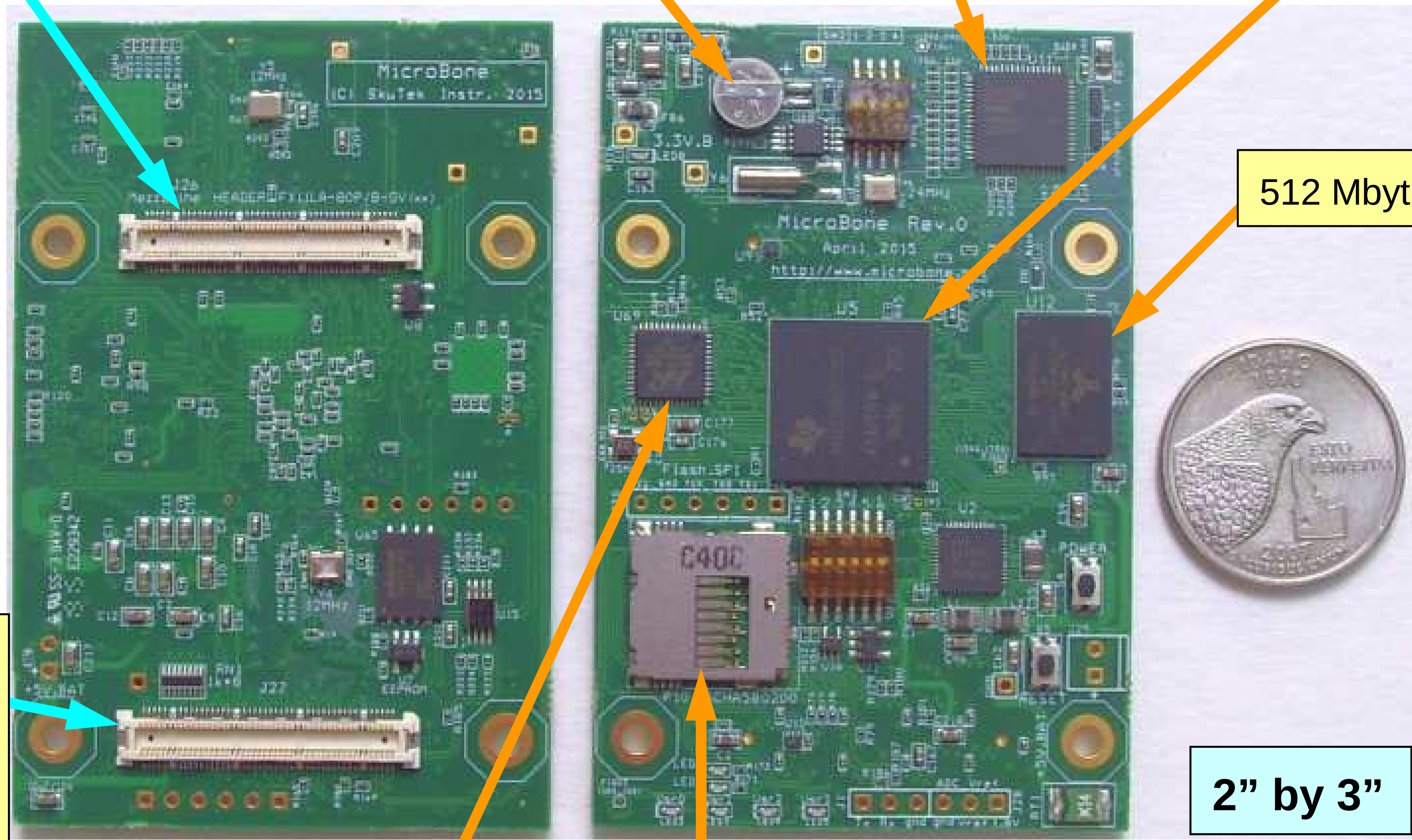
80-pin expansion connector A.
Memory interface, USB, video.

Real Time Clock with battery.

Video driver chip.
(Optional.)

1 GHz ARM with two
Programmable Real Time Units

512 Mbytes DDR3



80-pin expansion B.
Gigabit Ethernet, SPI, I²C.
Includes 8 analog pins:
12-bit ADC/DAC/GPIO

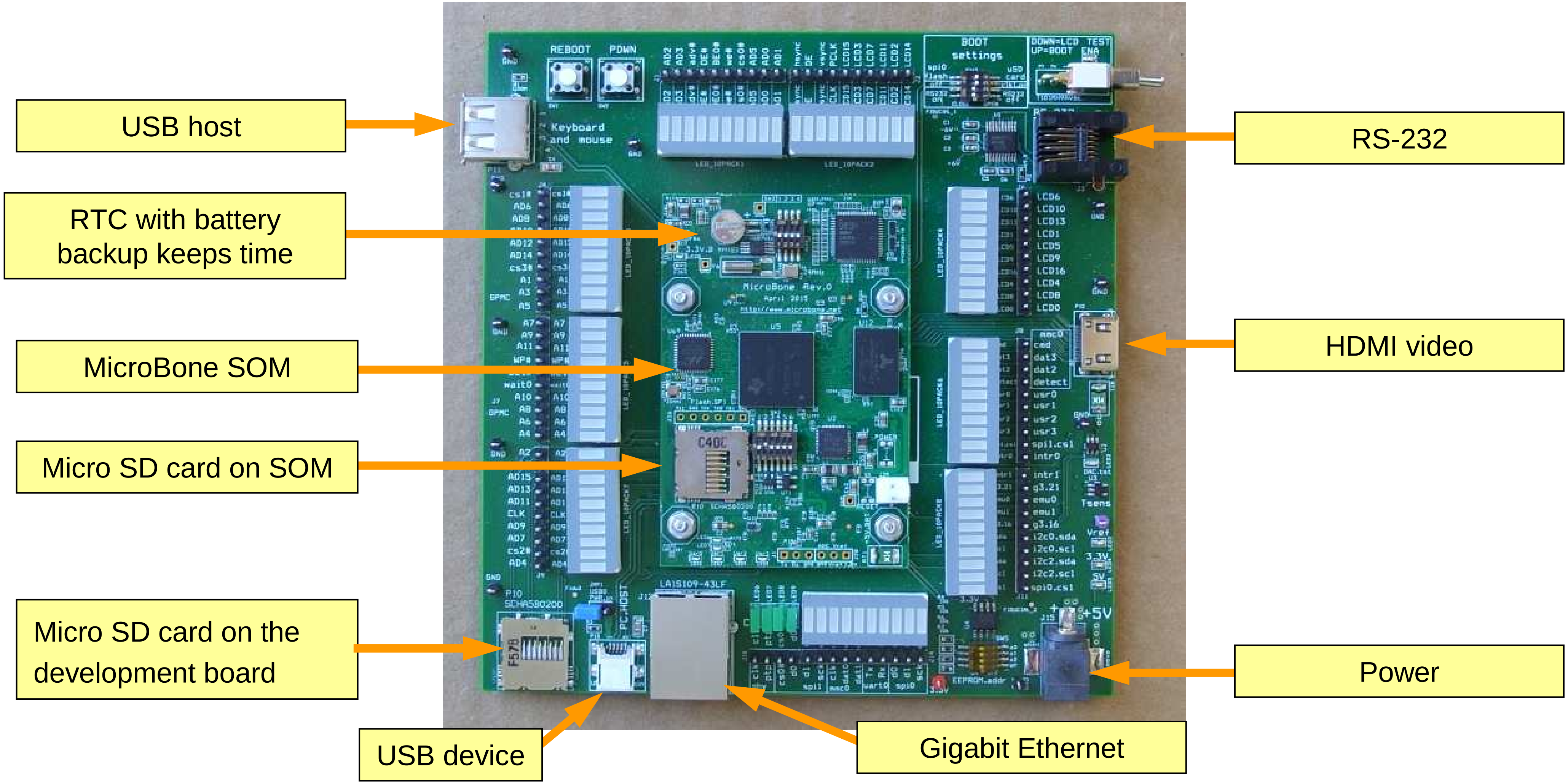
Gigabit PHY

Micro SD card

2” by 3”

MicroBone Development Board

- The SOM is hosted by a development board.
- The entire Linux is contained on the MicroSD card. The entire Linux can be upgraded **in 10 seconds**.
- The RTC with battery keeps track of the wall clock. (No need to call NTP…)
- Eight analog pins can be individually configured as 12-bit ADC, 12-bit DAC, or 5V-tolerant logic I/Os.



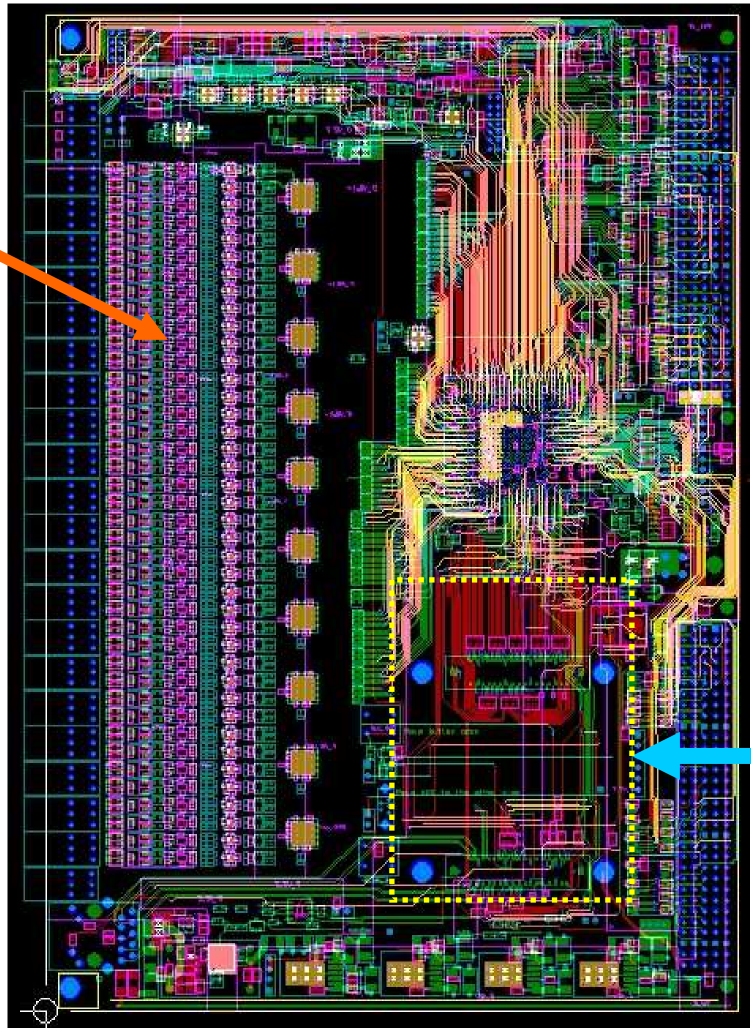
Benefit of the MicroBone: More ADC channels per board!

- Replacing the Blackfin circuitry with ARM System On Module allows to increase the number of ADC channels up to 40 (forty!).
- The 40-channel unit can be useful for silicon strip detectors, highly segmented HPGe detectors, or high channel count detector arrys.

X-ray view of the recent design file

40 channels
14 bits @ 100 MSPS

Input connectors
Dual LEMO



MicroBone SOM

Possible use for the embedded ARM: The Fog

The Industrial Internet of Things transforms isolated programmable devices into intelligent networks of connected machines. The <u>cloud</u> is a component in these systems, but it <u>is hardly primary</u>. The intelligent software that drives these systems must also reside in the field at the "edge." There is no time, bandwidth or reason to send the data from these devices to a data center. Instead, <u>the compute must come to the devices</u>.

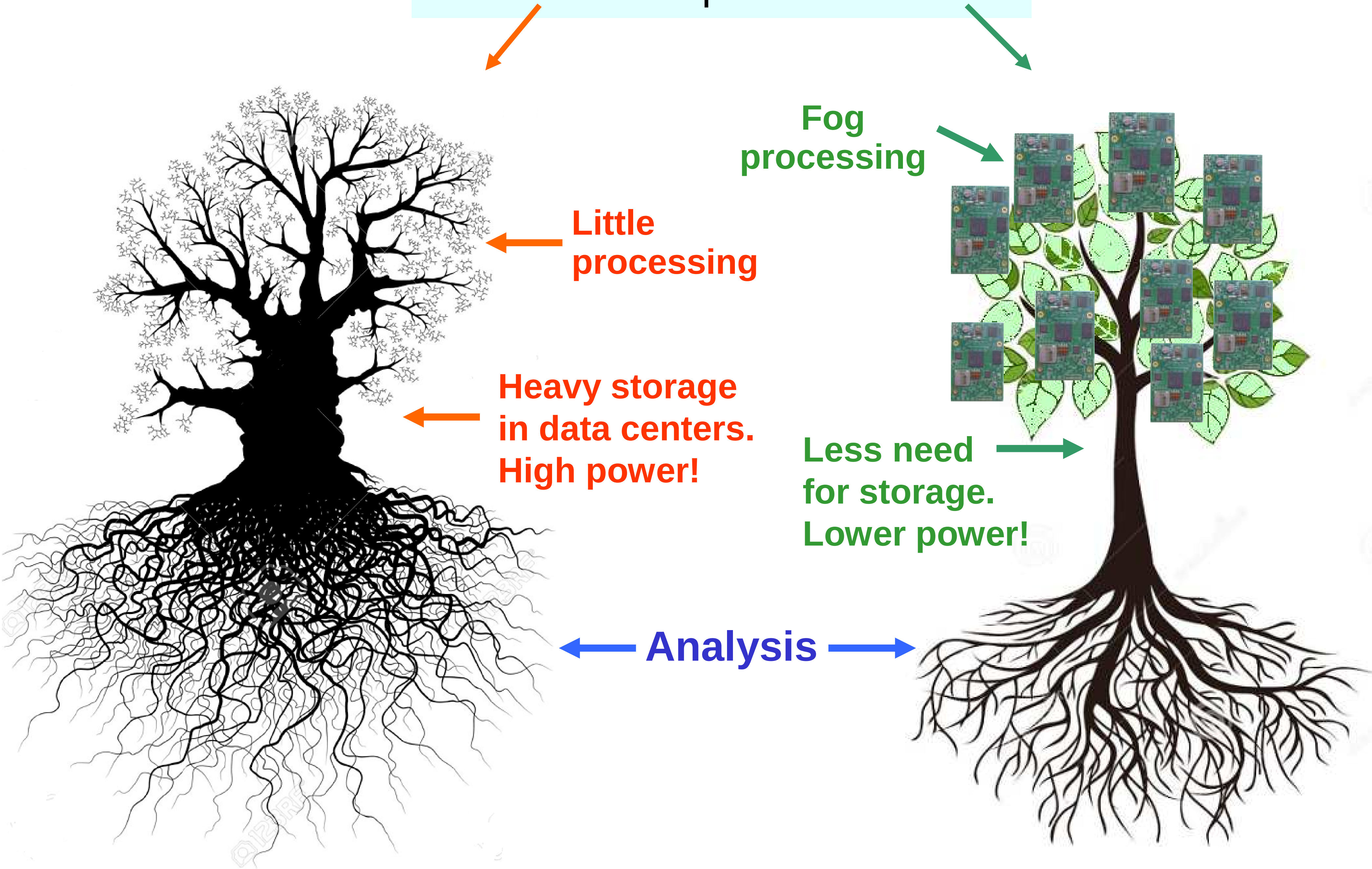
This design is called "fog computing."

Dr. Stan Schneider, CEO, RTI

- Do we have the bandwidth to **<u>always</u>** send **<u>all</u>** the data from the digitizers to a data center?
- Can we rather use computing power inside the DAQ modules?
- Can we find worthy tasks for embedded computing?
  - In-situ histogramming?
  - Waveform preprocessing?
  - Pulse deconvolution?
  - Local trigger calculations?
  - Signal quality monitoring?

Can Fog Computing reduce the need for storage?

Can **this** be replaced with this?

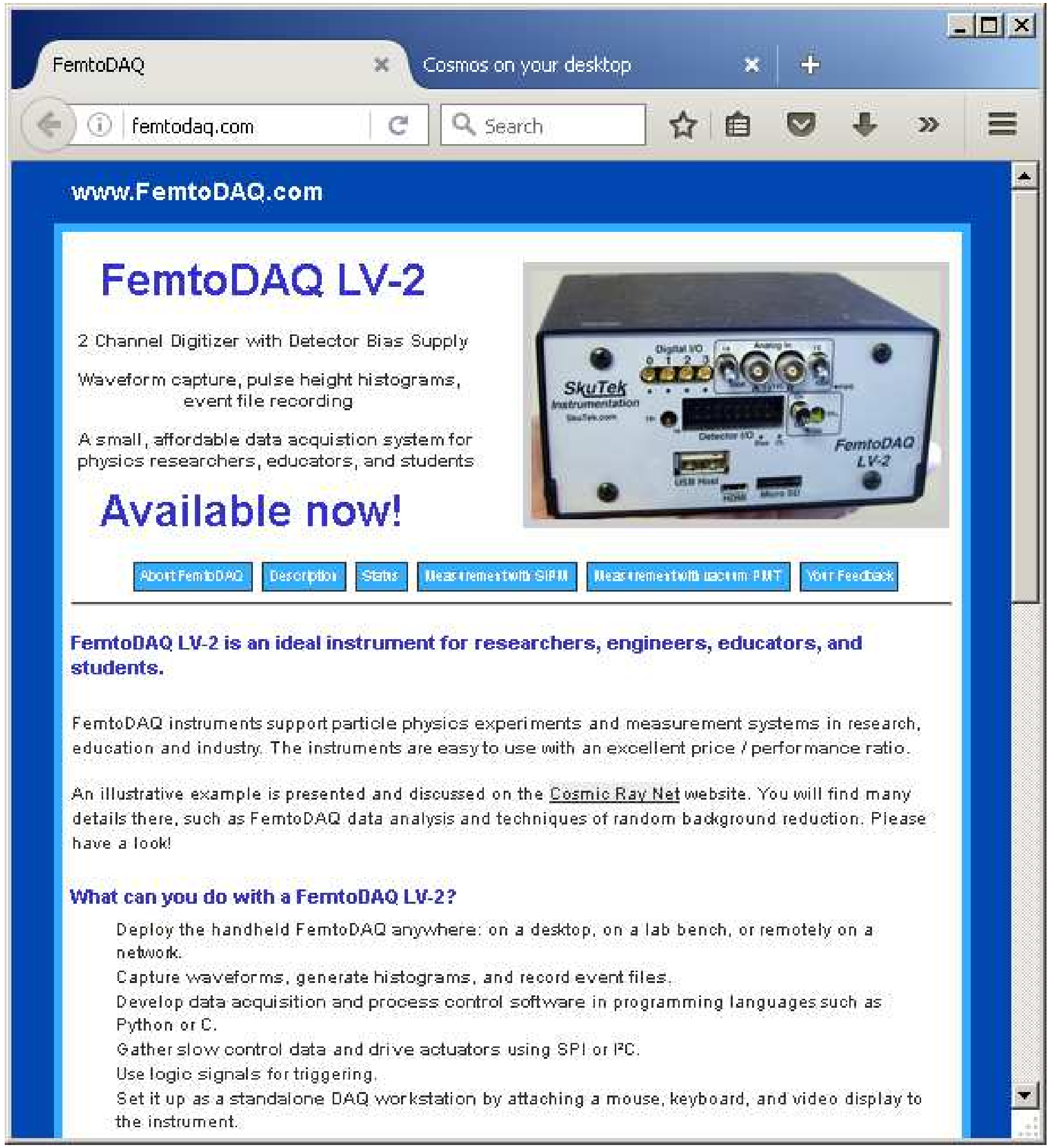


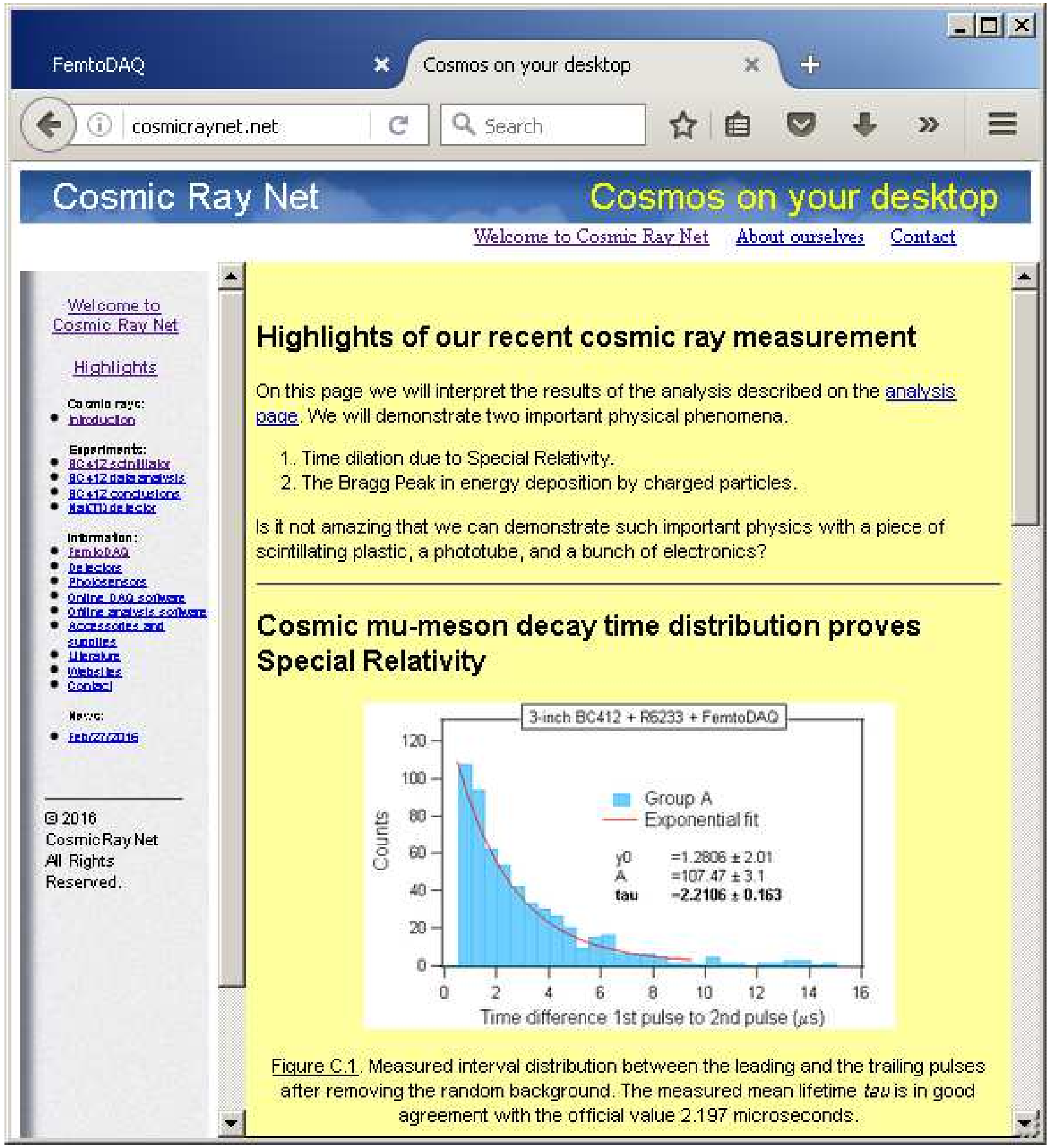
Low cost **ARM Fog Data Acquisition**

Dual channel FemtoDAQ with Silicon Photomultiplier control: an entry-level, low cost, easy to use DAQ.

Instrument: **FemtoDAQ.com**

Example application: **CosmicRayNet.net**





Summary

- We are developing a digital DAQ for the LUX-Zepplin detector with 1,359 channels.
- We developed custom data acquisition electronics for LUX-Zepplin.
  - 32-channel digitizer: 14 bits @ 100 MSPS.
  - Trigger / Logic module with 14 LVDS links and a gigabit Ethernet readout.
- We are now upgrading our electronics using the ARM processor and Kintex-7.
  - ARM will provide better performance in less space.
  - ARM can preprocess the events ("fog computing").
  - Kintex-7 provides more logic resources and a larger waveform memory than our present Spartan-6.
- Thanks to the reclaimed board space we are now developing a 40-channel digitizer.
- Powerful embedded ARM processors will enable *fog computing* which is offloading tasks from the Cloud.
- Adopting the *fog* approach can be valuable for the Nuclear Physics DAQ.
- Our inexpensive FemtoDAQ can become the development tool for the *fog* development.

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Backup slides

Improved CPU performance in numbers

- ARM has superior performance thanks to integration of many peripherals on chip.
- ARM will provide 4x more RAM with 3x higher nominal performance.
- NEON vector floating point unit and the Mobile GPU which can be used for event processing.
- Programmable Real Time Units (PRU) can be used for software trigger with deterministic latency.
- ARM will run mainstream Linux (Debian, Ubuntu, etc.) with up to date security features.

Feature	BF561 (present)	ARM AM335x (new products)	Improvement?
# cores	two	three (1 ARM + 2 PRU)	yes
Speed	2*600 MHz	1 GHz + 2*200 MHz	~same
Off-chip RAM memory	128 MB	512 MB	4x more
Type of RAM memory	SDRAM	DDR3	
Memory bus	133 MHz * 32 bits	400 MHz * 16 bits * 2 (DDR)	3x more
Separate SDRAM / SRAM buses	no	yes	yes
Floating point	no	yes	yes
USB-2 on chip	no	yes	yes
Gigabit MAC on chip	no	yes	yes
Graphics unit on chip (GPU)	no	yes	yes
Resident GUI	no	yes	yes
Linux version running on-board	uClinux	full Linux (Debian, Ubuntu, …)	yes
Linux community projects	few	many	yes

Improved FPGA performance in numbers

More logic, larger waveform memory

- Spartan-6 was the best tradeoff between price and performance circa five years ago.
- The new Kintex-7 FPGAs now offer more digital resources which we need for more channels.

Feature	XC3S5000 Spartan-3 a)	XC6SLX150 Spartan-6 b)	XC7K325T Kintex-7 c)	XC7K410T Kintex-7 c)	Relative to XC3S5000
Equivalent logic cells from Data Sheet	74,880	147,443	326,080	406,720	2.0 / 4.4 / **5.4**
Multiply-accumulate units	104 d)	180	840	1540	1.7 / 8.1 / **14.8**
Waveform memory (k samples) e)	104 k	268 k	890 k	1,590 k	2.6 / 8.6 / **15.3**
Balls per package	900	900	900	900	same
I/O pins	633	576	500	500	0.9 / 0.8 / 0.8
Price lowest speed grade (900 balls)	$166	$210	$1,032	$1,496	1.3 / 6.2 / 9.0
Price “our” speed grade (900 balls)	$191	$210	$1,550	$1,796	1.1 / 8.1 / 9.4
$$ per channel for 40 channels f)	$4.8	$5.3	$39	$45	

a) XC3S5000 is used in present GRETINA digitizers. It is the community’s performance yardstick.

b) XC6SLX150 is used in our present 10-channel and 32-channel digitizers.

c) These pin compatible Kintex-7 chips will be used in our forthcoming high density digitizers (40 channels).

d) XC3S5000 provides multipliers without the built-in accumulate register.

e) Total number of block RAM bits divided by 18. Parity bits are considered not useful for waveform storage.

f) FPGA cost per channel for “our” speed grade and 40 channels.