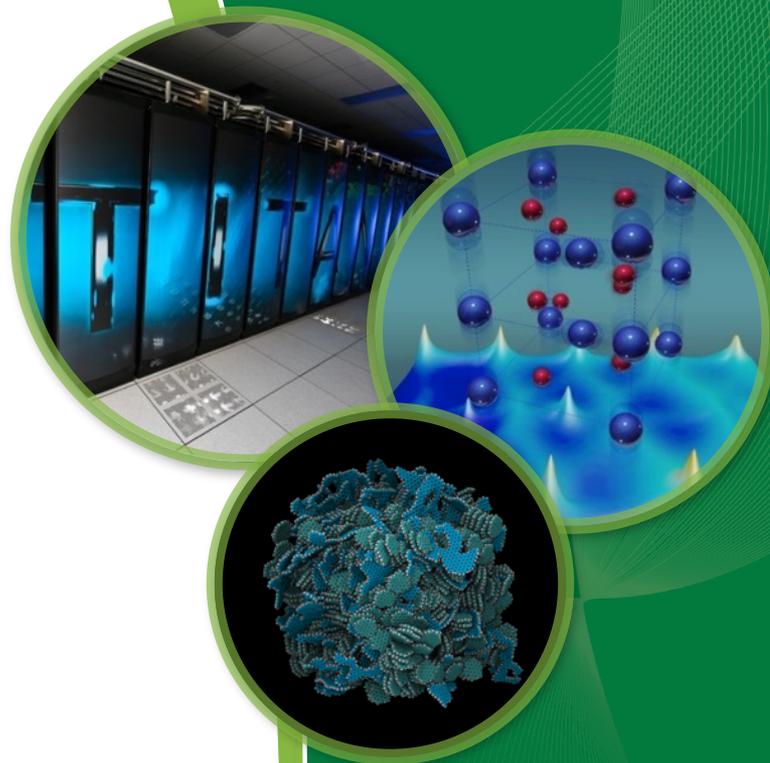


Timing panel - Plans

Robert Varner



Charge to the Timing Panel - Foreword

- The Timing Panel is formed to understand the timing needs associated with the running of experiments at FRIB.
- “Timing” is a general term that encompasses **numerous aspects** of data acquisition. This term is used not only to define **interactions between elements** of a given detector (e.g. triggering and channel alignment) but also information that a given detector’s **DAQ may need from the accelerator** (e.g. interaction delay with respect to RF bunch).
- The low-energy community also has a long history of using multiple, complimentary detectors designed by different groups to perform simultaneous measurements of different interaction signatures (e.g. alpha-gamma coincidences).
- In experiments that use multiple, coupled detectors like this, the term “timing” also expands to mean the correlation of data from multiple detector DAQ systems to identify linked events.

Charge - Text

The Timing Panel shall **research timing and synchronization** aspects of detector-accelerator and detector-detector communication based upon the information provided from each detector group about their detector system. The Panel thus has a three-part charge:

1. Identification of **all timing information data flows** required within the foreseeable detector configurations that will run at FRIB including both accelerator-to-detector and detector-to-detector. This includes timestamps, reference pulses, clock signals, safe crossing of clock domains, etc.
2. Enumeration of the **current and foreseeable technologies** available for the distribution of timing information, and evaluation of how well each technology services the identified needs.
3. Development of a report **recommending the appropriate subset of technologies** sufficient to ensure that all identified timing information data flows will be available to experimental campaigns at FRIB.

Charge - Specific Considerations

- The Data Acquisition Working group has identified specific items that the Timing Panel should include in their deliberations:
 - The panel is requested to consider the wide variety of detector systems in use in the low-energy community and the disparate needs and requirements of the many experimental groups.
 - How separate the physical distribution of timing information should/can be from data acquisition network infrastructure.
 - An estimate of the cost to procure, install and operate the necessary infrastructure required to implement the recommendations of the panel.

Timing panel - technical options

- **Clock-only source fan-out to systems**
 - S800 + CAESAR, many other examples
- **GPS**
 - clock in every system
- **High speed serial links**
 - *Synchronous Data Stream*
 - measures propagation delays - synchronize clocks
 - send priority commands to systems - triggers, status, run control, setup
 - *Embedded clock*
 - MyRIAD and Gretina timing system
 - MRF timing system planned for FRIB
 - *Ethernet*
 - White Rabbit
 - Other Variations of PTP IEEE 1588v2

From John Anderson in 2015

Clock-only versus a synchronization data stream

- All SERDES-based clock distributions allow for synchronous data transmission to all receivers
- Numerous uses for synchronous data in addition to clock
 - Synchronous resets/sync pulses allow for localized time-stamps on all data captured – greatly simplifies event collection & sorting.
 - Multiple trigger decision frames per cycle provides triggering flexibility
 - Synchronous *commands* simplify data quality monitoring by allowing measurement of parameters such as event rates at exactly the same time in all data sources.
 - Synchronous *commands* can also simplify calibration by causing pedestal/baseline measurements in all channels at the same time
- The DGS/Gretina command frame format has evolved to support all these features and is a currently existing, robust solution.
- **All SERDES links are by nature bi-directional, providing a natural technique for error collection, trigger formation or flow control.**



Based on discussion with Sean Liddick

Synchronization of DAQs

- Two scenarios that would be considered separately.
 - Event level synchronization
 - Just need multiple systems close enough in time to build events ~10-100 ns.
 - TOF level synchronization
 - Synchronization good enough to reconstruct a time-of-flight, ~10 - 100 ps.
- System needs to be
 - Flexible
 - Extendable
 - Stable
 - Easy to setup (< 2 hrs)
- Trigger?

Event level synchronization

- Common distributed clock of ~ 50 MHz.
- Central source of “RUN”, “STOP”, and “TIMESTAMP CLEAR” signals.
- Suggested protocol
 - All subsystems should be able to:
 - Accept input clock up to 50 MHz and be able to count it in a latching scaler of at least 48-bit depth.
 - Accept a “RUN” signal.
 - Accept a “STOP” signal.
 - Accept a “TIMESTAMP CLEAR” signal.
 - Provide “READY”

Event level synchronization

- Sequence of steps
 - Clocks distributed
 - If subsystem not RUNNING then ignore signal
 - If subsystem RUNNING count clock cycles and increment latching scaler (48-bit minimum).
 - Accept “TIMESTAMP CLEAR”
 - Reset counters
 - Accept “RUN”
 - Start counting clock cycles and incrementing scaler.
 - Accept “STOP”
 - Stop counting clock cycles.
- Keep in mind the “RUN” signal doesn’t have to be linked to data taking.
- AND of all subsystem “READYs” required before “RUN”.
- Centralized hardware source for “TIMESTAMP CLEAR”, “RUN”, and “STOP” signal. There will be offsets between systems but they should be *known and stable*.

TOF level synchronization

- Event timing solutions exist
 - MyRIAD and DGS modules (150ps jitter already)
 - MRF timing (FRIB accelerator) may be sufficient
 - need to understand it better
- Can we do something awesome?!
 - 10 to 100 ps precision is cutting edge, but not crazy
 - Clocks in phase to 10ps precision allow physics measurements.
 - Time of flight for neutrons?
 - Time of flight for beam from fragment analyzer to target?
 - System-wide trigger formation in software!
- World class technology for a world class facility.

Panel Members

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Sean Liddick (NSCL)

John Anderson (ANL)

Schedule

- Work starts now
- Meetings every other week we know how this will work.
- Report by January 2017

What does the community want

- Timestamps or clock ticks
- Connect through
 - VME modules
 - PXI modules
 - PCI cards
 - uTCA cards
 - Ethernet
- What resolution clock? How many ticks per second?
- What commands?
- What other information?