

FRONT-END MODULE READOUT AND CONTROL ELECTRONICS FOR THE PHENIX MULTIPLICITY DETECTOR

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Front-end module (FEM) readout and control are implemented as modular, high-density, reprogrammable functions in the PHENIX Multiplicity Vertex Detector. FEM control is performed by the heap manager, an FPGA-based circuit in the FEM unit. Each FEM has 256 channels of front-end electronics, readout, and control, all located on an MCM. Data readout, formatting, and control are performed by the heap manager along with 4 interface units that reside outside the MVD detector cylinder. This paper discusses the application of a generic heap manager and the addition of 4 interface module types to meet the specific control and data readout needs of the MVD. Unit functioning, interfaces, control timing, data format, and communication rates will be discussed in detail. In addition, subsystem issues regarding mode control, serial architecture and functions, error handling, and FPGA implementation and programming will be presented.

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