

# A DISCRIMINATOR WITH A CURRENT-SUM MULTIPLICITY OUTPUT FOR THE PHENIX MULTIPLICITY VERTEX DETECTOR

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A current output multiplicity discriminator for use in the front-end electronics (FEE) of the Multiplicity Vertex Detector (MVD) for the PHENIX detector at RHIC has been fabricated in the a 1.2- $\mu\text{m}$  CMOS, n-well process. The discriminator is capable of triggering on input signals ranging from 0.25 MIP to 5 MIP. Frequency response of the discriminator is such that the circuit is capable of generating an output for every bunch crossing (105 ns) of the RHIC collider. Channel-to-channel threshold matching was adjustable to  $\pm 0.05$  MIP. One channel of multiplicity discriminator occupied an area of 85  $\mu\text{m}$  x 630  $\mu\text{m}$  and consumed 515  $\mu\text{W}$  from a single 5-V supply. Details of the design and results from prototype device testing are presented.

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