

# DEVELOPMENT OF FRONT END CONTROLLER/HEAP MANAGER FOR PHENIX

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A controller/heap manager has been designed for applicability to all detector subsystem types of PHENIX. The heap manager performs all functions associated with front end electronics control including ADC and analog memory control, data collection, command interpretation and execution, and data packet forming and communication. Interfaces to the unit consist of a timing and control bus, a serial bus, a parallel data bus, and a trigger interface. The topology developed is modular so that many functional blocks are identical for a number of subsystem types. Programmability is maximized through the use of flexible modular functions and implementation using field programmable gate arrays (FPGAs). Details of unit design and functionality will be discussed with particular detail given to subsystems having analog memory-based front end electronics. In addition, mode control, serial functions, and FPGA implementation details will be presented.

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