

DESIGN AND PERFORMANCE OF BEAM TEST ELECTRONICS FOR THE PHENIX MULTIPLICITY VERTEX DETECTOR

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The system architecture and test results of the custom circuits and beam test system for the Multiplicity-Vertex Detector (MVD) for the PHENIX detector collaboration at the Relativistic Heavy Ion Collider (RHIC) are presented in this paper. The final detector per-channel signal processing chain will consist of a preamplifier-gain stage, a current-mode summed multiplicity discriminator, a 64-deep analog memory (simultaneous read-write), a post-memory analog correlator, and a 10-bit 5 μ s ADC. The Heap Manager provides all timing control, data buffering, and data formatting for a single 256-channel multi-chip module (MCM). Each chip set is partitioned into 32-channel sets. Beam test (16-cell deep memory) performance for the various blocks will be presented as well as the ionizing radiation damage performance of the 1.2 μ m n-well CMOS process used for preamplifier fabrication.

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