

A MONOLITHIC, CONSTANT-FRACTION DISCRIMINATOR USING R-C DISTRIBUTED DELAY LINE SHAPING

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A monolithic, CMOS, constant-fraction discriminator (CFD) was designed and fabricated in a 1.2- μ , N-well process. This circuit used an on-chip, distributed R-C delay line to realize the constant-fraction shaping. The delay line was constructed of a 4.8- μ wide, 500- μ long serpentine layer of polysilicon above a grounded second layer of polysilicon. This line generated about 1.1 ns of delay for a 5-ns risetime signal with a slope degradation of only 15%. The CFD also featured de feedback for both the arming and zero-crossing discriminators to eliminate timing errors caused by offsets. The entire circuit, including the delay line, required an area of 200 μ x 950 μ . The timing walk for 5-ns risetime signals over the dynamic range from -20 mV to -2 V was less than ± 150 ps. Each channel of the CFD consumed similar to 15 mW from a single 5-V supply.

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