THE PHENIX MUON IDENTIFIER FRONT END ELECTRONICS

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The MUID Front-End Electronics (FEE) must convert the anode pulses from the panels' Iarocci tubes into a bit string. This data is used in the level-1 trigger decision, and for accepted events this same data is written onto mass-storage media. A block diagram of the MUID data flow is shown in Fig. 1.

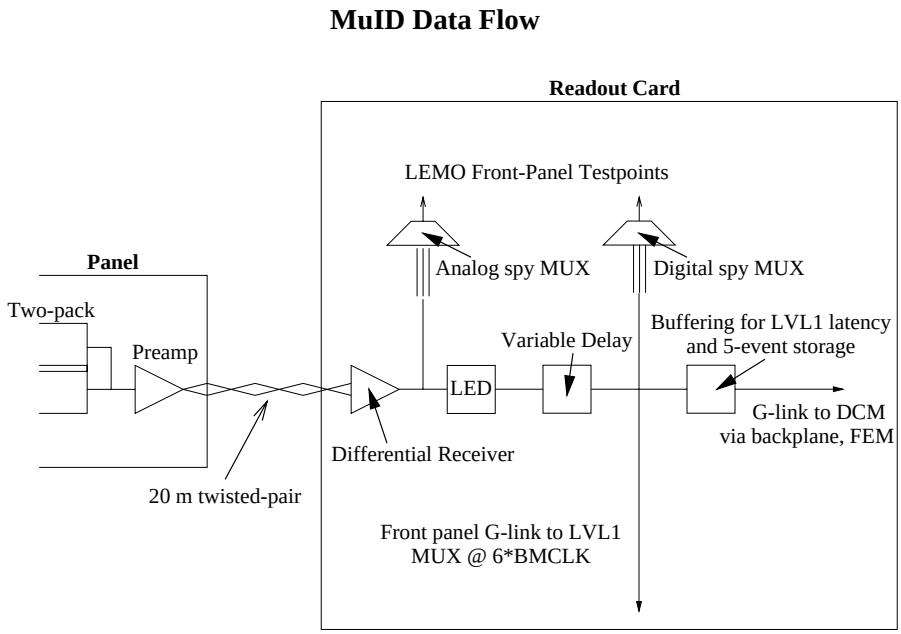

Figure 1: Block diagram of the MUID FEE readout scheme.

The first piece of the MUID FEE, inside the panels, is a board that distributes high voltage to the streamer tubes and amplifies the signals by $\sim$100, driving them differentially on long, twisted-pair cables to crates of processing electronics. A schematic showing all communication to and from the these crates is shown in Fig. 2. The physical architecture of the crates is shown in Figs. 3 and 4. There are four such crates for the MUID.

Each slot in a crate (except one) contains two 96-channel boards — a Transition Card (TC) and a Readout Card (ROC). Amplified differential signals from the panels enter the back of the crate via the TCs to ease replacement of defective ROCs. Each ROC is connected to the corresponding TC through a custom pass-through backplane. On the ROCs the signals are amplified further, discriminated, passed though a novel programmable delay circuit and latched. The latched bit pattern is immediately sent to the level-1 trigger via optical fiber (one per ROC). The ROC has an event FIFO to provide a level-1 trigger latency buffer for all events and further buffering of level-1 accepted events to conform to the PHENIX pipelined, dead-timeless architecture. The ROCs also have several diagnostic features — a maskable pulser to test bit patterns and front-panel analog and digital "spy muxes" to allow *in situ* examination of board behavior.

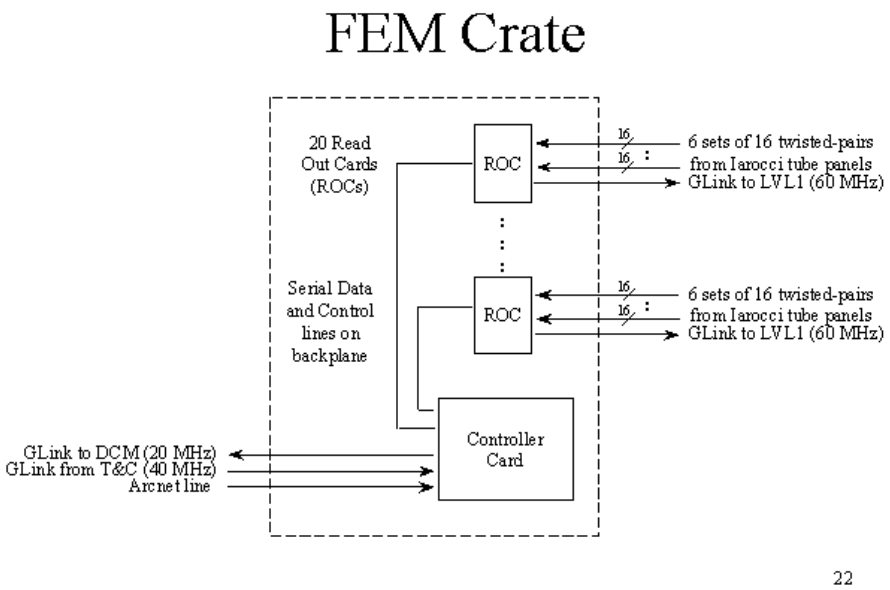

Figure 2: The MUID FEE communication links.

A Front-End Module (FEM) occupies the final slot in each crate. The FEM collects and formats the latched bit patterns from the 20 ROCs in its crate. It also provides the interface between the ROCs and the PHENIX on-line and data acquisition system. The FEM has three connections to PHENIX:

An ARCNet connection for downloading the FEE configuration — FPGA programs, threshold and delay settings, mux and mask selects.

An optical G-link connection to a Data Collection Module — the next step on the way to recording events on tape, and the first common to all PHENIX subsystems.

An optical G-link connection to a Granule Timing and Control Module — the source of synchronization, operating mode selection, and the level-1 trigger select signal.

The FEM and ROCs in a crate are connected by a custom VME-based backplane that incorporates geographical addressing to allow communication to (serial control) and from (data collection) individual ROCs.

In the past year the in-panel amplifier/HV distribution cards were designed, prototyped, fabricated, and installed in the MUID panels. In addition, we reached a mature state in the system design and prototyping of the crate electronics. Prototypes of the crate, the two custom backplanes, and the TCs are in hand. A one-channel ROC prototype was fabricated to test the receiver and discriminator. An 8-channel ROC prototype, that allows signal input through a TC and which uses a more realistic layout, was fabricated to test a multichannel version of this analog circuitry and to test the variable delay, mux select, and mask select circuitry, see Figs. 5 and 6. The analog circuitry (pulser, analog mux, discriminator) behaves well with a pulse generator (high common mode rejection ratio, low

cross-talk, good signals at the analog mux, and the discriminator input). All digital circuitry, including the variable delay, looks good. We are currently retrofitting the full-scale prototype panel at ORNL with production versions of the amplifier/HV distribution boards to test the complete system performance. Finally, schematics for fully functional ROC/FEM prototypes are far along.

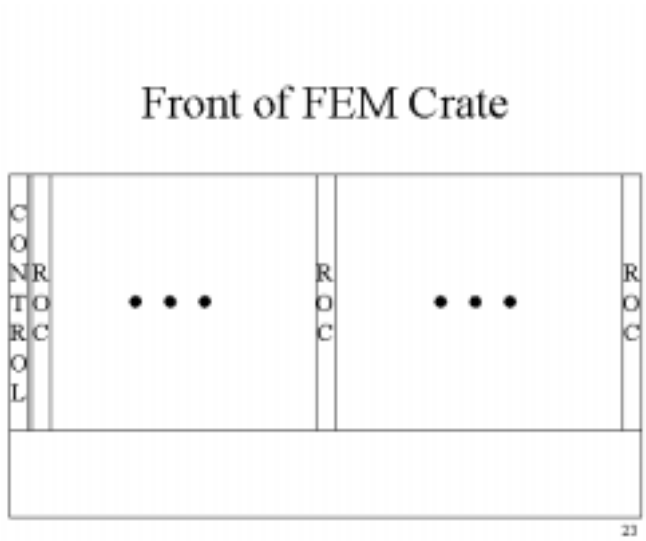

Figure 3: Front view of a MUID FEE crate.

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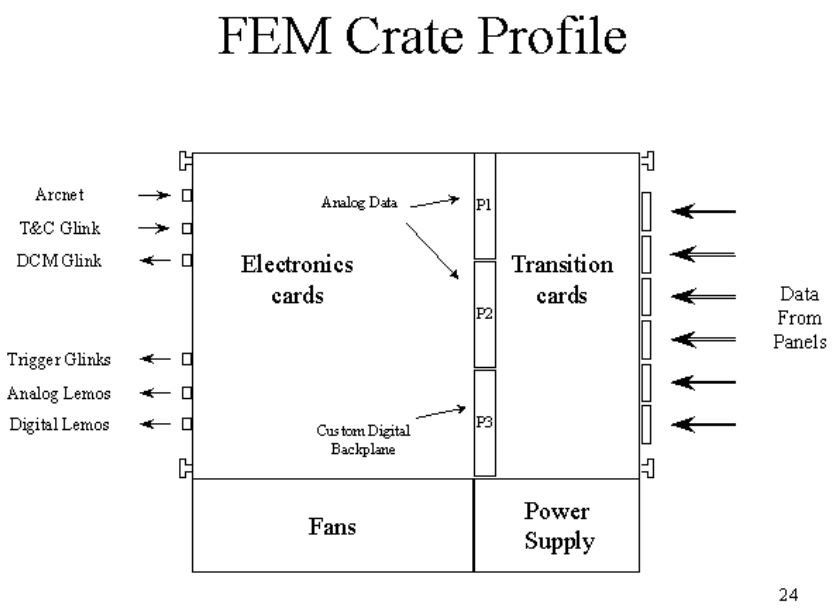

Figure 4: Side view of a MUID FEE crate.

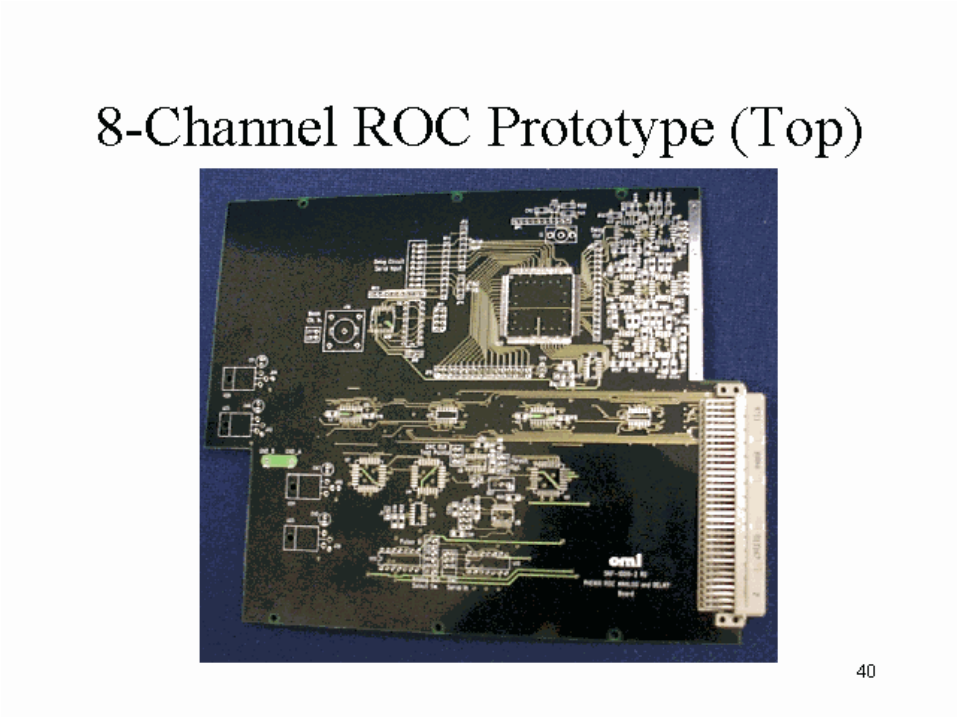

Figure 5: Front of the eight-channel ROC prototype.

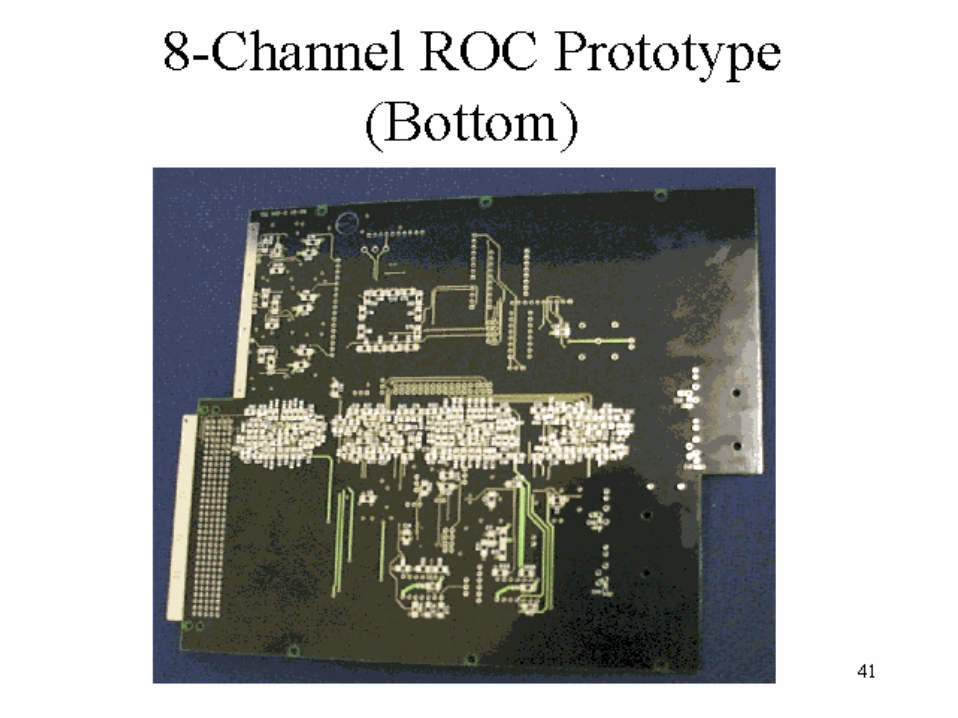

Figure 6: Back of the eight-channel ROC prototype.