PHENIX MUON TRACKER FRONT-END ELECTRONICS

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The PHENIX Muon Tracking chambers are large, multiwire proportional chambers with two methods of readout. Fine position information is obtained from interpolation of charge measured on 1-cm-wide cathode strips oriented perpendicular to the anode wires of the chambers. Position resolutions better than 150 microns are expected based on prototype chamber measurements with particles. Coarse position information for the orthogonal coordinate is obtained from the anode wires themselves. The anode wires are strung in a series of chords across the chamber that are tangent to circles centered on the RHIC beam axis. There are 8 or 16 such chords in Station 1 and 2/3. The anode wires are spaced radially 1-cm apart. The cathode strips are etched on both cathodes of each chamber, 0.5-cm wide, with each second strip read out. One set of strips is perpendicular to the anode wires for each station layer, and the other is set at a stereo angle between $\pm$11.25 degrees, depending on z-position of that chamber layer. The stereo angles were chosen based on both pattern recognition and cathode construction considerations.

The electronics for the anode readout closely follows that for the Muon Identifier, discussed elsewhere in this report.

The electronics for the cathode strips uses a processing chain consisting of a charge-sensitive preamplifier, a shaping amplifier with 700-ns peaking time, and the AMUADC32 ASIC described elsewhere (under MVD FEE) to provide analog storage for LVL-1 trigger latency and multiple-pending-trigger readout plus an ADC for conversion to digital form. The preamplifier–shaper are implemented as an 8-channel ASIC which was prototyped during late 1997 and tested during 1998. This ASIC includes a preamplifier with 4-mV/fC sensitivity; a two-stage shaping chain using the same RHIC4B amplifier used in EMCal, RICH, and MVD; a maskable/settable charge-injection pulser for each channel; and serial download/readback control for remote programming. The chambers produce 80 fC most-probable charge, and allowance is made for up to ten times this charge output to allow for the Landau-tail of charge deposited in the chamber gas. The peaking time of 700 ns is for 0 pF load; this slows to 900 ns for 50 pF and 1100 ns for 200 pF external load, which roughly spans the range of strip capacitances to be encountered. The noise specification was 0.8 fC; better than 0.5 fC rms was achieved. The integral nonlinearity measured at the initial choice of biasing point is better than 0.5%, which meets the system requirements. The first-round prototype requires two small changes to correct metallization problems in the chip layout plus one series resistor change to improve power supply rejection ratio performance. These changes are underway.

A system concept for the MuTR Fee was developed at ORNL by J. Halliwell and M. Musrock. This consisted of 128-channel FEM crates with 64-channel readout boards hooked to the chambers by short lengths of twisted-pair cable. Control logic and communication to the PHENIX timing, serial, and data collection systems were modelled on the EMCal system, with removal of the trigger links. Responsibility for this part of the MuTR FEE was taken over by LANL and has since been developed into a full design for the mounting crates, backplanes, mechanical and electrical infrastructure, and services

routing. The PHENIX-generic ARCnet board will be used for serial communication, and a concentrator built to link MuTR FEM crates to a few central points where optical links to PHENIX timing and data collection electronics will sit. Schematic design of the two main FEM cards, namely, the cathode readout card which includes the above two ASICs plus links to the chamber electrodes, and the control card which has all state machine, list manager, and interface logic, is ongoing presently at LANL.

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