PHENIX RING-IMAGING CERENKOV FRONT-END ELECTRONICS

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The PHENIX Ring-Imaging Cerenkov (RICH) counter is instrumented with 5120 fast photomultiplier tubes arranged to cover the focal-plane of the detector with a (nearly) hexagonal close-packed array. The focal plane is curved to follow the optics of the counter, as determined by the sectioned spherical mirrors used to form the image. The gas used as radiator will be either ethane or carbon-dioxide. Both produce about 15-20 photoelectrons from the ring of Cerenkov photons imaged onto the PMT array. The PHENIX RICH is designed as an electron/positron tagger and thus has its threshold set at a Lorentz-gamma of about thirty. This helps keep unwanted pions, kaons, and other hadrons below threshold but does mean that there are few photoelectrons produced at the image on the focal plane. The PMTs used are, therefore, selected to have good single-photoelectron resolution. A preamplifier with gain of ten, designed and built at the University of Tokyo with some ORNL design assistance, is used as the initial stage of the electronics processing chain. These preamps have been produced and are installed along the wall of the large RICH pressure vessel produced by Florida State University.

The remaining electronics follow closely the design of the EMCal front-end electronics. The major difference is the lack of a second (high-)gain stage due to the much smaller dynamic range of pulse-heights produced by the RICH compared to the EMCal. The RICH processing chain thus consists of the following functions, implemented in two separate ASICs. The first ASIC, known as Int-R, includes an integrator stage (modeled on the one used successfully for WA98 electronics), a variable-gain amplifier, a final-stage amplifier, a LED/CFD timing discriminator, a TAC, 2x2 current-summers used as trigger circuits, serial setup/readback for programmable control of the chip, and a mux circuit for analog monitoring of chip performance at various internal stages. The Int-R is built as an 8-channel ASIC using ORBIT's 1.2 micron N-well CMOS process. The second ASIC is the AMUADC32 described above under the MVD electronics write-up and includes the 64-cell-deep analog-memory unit, used for LVL-1 delay and digitization staging, and the ramp-type ADC unit used to digitize each channel. This ASIC has 32 channels and was fabricated in HP's 1.2 micron N-well CMOS process.

The AMUADC32 chips have been produced and tested. The Int-R chips have been produced as part of a larger prototyping run. Nearly all functions of the Int-R have been tested as of this writing. The prototype run they were part of produced enough of them to satisfy full production requirements. Testing will be completed during spring 1999.

The control logic, serial logic, trigger logic and board design for the RICH are all modeled on the operating EMCal design. ORNL has consulted on all aspects of this design. Final design, board layout and prototype construction are being carried out at the University of Tokyo, Nagasaki Institute of Applied Science, and Waseda University, Japan. Initial prototypes have been produced for all boards plus the custom interconnecting backplane, with good testing results. The next prototypes will use the production versions of the two

ASICs noted above and should be prepared by summer 1999 for testing. Final production will follow in Japan.

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