PHENIX PAD CHAMBER FRONT-END ELECTRONICS

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The PHENIX spectrometer has three layers of non-projective tracking chamber in each of the two Central Arms. These so-called pad chambers are located just after the inner Drift Chamber (DC), which provides precision momentum determination, and just before and after the Time Expansion Chamber (TEC), which provides tracking and particle-ID at large radius. The DC has stereo wires but requires one layer of non-projective tracking to determine the non-bend coordinate and resolve ambiguities, and the TEC is purely projective and thus must operate in conjunction with chambers giving space-points. The first two layers of Pad Chamber also bracket the Ring-Imaging Cerenkov Counter (RICH), providing that device with entry and exit coordinates of candidate electron/positron tracks. These space points can be used to help determine direction cosines, which are then matched to the directional information provided by the RICH.

The Pad Chambers are built as very thin panels. The central volume is loaded with argon-ethane gas and strung with cathode wires and with anode wires, which create the primary signals by amplifying charge liberated by passing charged particles. The gas volume is enclosed between two large area electrodes, one of which is etched into a fine-grain interpolating pixel pattern. A proportional avalanche on the anode wire induces signals on several of the nearest pixels. There are over 1.8 million pixels, which are grouped into sets of 9 to form signal pads connected to readout electronics. The pads are interleaved using a novel design in order that one particle induces a signal on 2 or 3 pads, allowing some position interpolation plus greatly improved pattern recognition. The system has over 207 thousand pads and thus electronics channels, necessitating development of a low-cost, low-radiation-length, and low-power electronics chain.

The signals are first integrated and amplified in a charge-sensitive preamplifier. This has a gain of 10 mv/fC, matched to the most-probable signal sizes of 20-40 fC. The innermost layer is thinner than the outer two pad chamber layers and produces proportionally smaller signals. The preamplifier output is then discriminated and converted to a pseudo-differential current output. This output is transmitted to a digital buffer which is clocked at 10 MHz, the nominal bunch-crossing frequency of RHIC. This buffer provides data memory, LVL-1 trigger latency delay, and triggered readout of the resulting data. These processing electronics are all located on a thin (100 microns) polyimid readout card (ROC) located directly above the relevant pixels and just outside the chamber gas volume. One readout card processes 48 channels. One chamber section has 45 ROCs, and there are 96 chamber sections total. Groups of 45 ROCs on one chamber section are read out in turn by a Front-End Module (FEM) located on the outermost Z-edge of the chamber section.

The TGL98v2 preamplifier-discriminator is implemented as a 16-channel ASIC manufactured in ORBIT's 1.2-micron n-well CMOS process. Each channel includes a charge-sensitive preamplifier with gain 10 mV/fC, an R-C coupled differentiating stage, a differ-

ential current source to drive the output, and a settable, maskable charge-injection pulser. Serial download and read-back are included for remote set-up of parameters. Three separate bias supplies are used: one for analog, one for the first discriminator stage, one for the balance of analog and digital circuitry. Considerable attention was given to proper biasing conditions, avoidance of double-pulsing, and recovery-time from large (more than 10x nominal) input pulses. The charge injection, integrator fall-time, channel-active mask, and discriminator threshold are among the items which are programmable via serial setup. A low-power design using less than 10 mW/channel was required due to limits on power usage over the exposed area of the Pad Chambers.

The TGL98 is followed by a Digital Memory Unit designed at SiCon in Sweden and fabricated at AMS in Austria. It includes 48 channels of digital delay line (shift-register) and thus can service three TGL98 ASICs. The DMU is clocked at 10 MHz, the nominal RHIC bunch-crossing frequency. It receives LVL-1 accept commands and prepares the "OR" of anywhere from one to eight most recent crossings for output, on a channel-by-channel basis. Its output is by differential serial lines which transmit up to 2 meters across the motherboards to receivers on the FEM cards.

One ROC includes thus three TGL98 and one DMU, plus associated line transceivers and biasing components. It is implemented as a 2-layer circuit card built on 100-micron-thick polyimid. Connection to the chamber is by a small connector card of similar construction which has actual wiring to the pixels and includes some of the clock and power-handling circuitry. By separating the ROC and connector cards, the actual chamber construction time line could be largely separated from the ASIC and ROC production time line, giving flexibility in meeting schedules. Both the connector card and ROC were designed and made by Lund University.

Both the motherboard, which carries all signal traces between the ROCs and FEMs, and the pixel board, which has the signal electrodes in the chamber proper plus associated output traces, are built as standard clad circuit boards, albeit very large, thin ones with many thousands of plated-through holes for signals to reach from pixel to preamp. These boards are up to 2 meters in size. Mechanical support is given by honeycomb panels placed between the circuit boards and made by Hexcel. The entire arrangement must be gas-tight to keep the operating chamber gas oxygen-free.

The front-end module card is mounted on the outer Z-edge of the chambers and is a standard multilayer circuit card. It includes all transceiver logic to move signals between itself and the ROCs, all power conditioning electronics for itself and the ROCs, fusing, fiber-optics links to the PHENIX timing and data-collection systems, an ARCnet connection to the PHENIX central FEE serial-control system, and power inputs from the low voltage power system. Its main active components are a set of field-programmable gate arrays which buffer and sort the outputs from the DMUs, receive, stack up and buffer multiple LVL-1 accept requests, format and output data from the chamber to the main PHENIX data acquisition system, handle all state-machine operations, handle much of the serial communication to the ROCs, and handle initialization of the entire electronics chain. The full system requires 96 FEMs, each of which services 2160 channels of detector.

The entire system has been tested extensively over the past year. A full-scale prototype chamber has been fully instrumented and operated at full speed using pre-production prototype electronics. Several million events in succession have been handled properly.

Threshold control, efficiency for minimum-ionzing particles, and uniformity of response have all met requirements. The components are all in full production for installation into RHIC during 1999.

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