FRONT END ELECTRONICS FOR THE PHENIX MULTIPLICITY-VERTEX DETECTOR

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The Multiplicity-Vertex Detector in the RHIC PHENIX experiment is designed to measure charged-particle multiplicity, as a function of pseudorapidity and azimuth, event-by-event in collisions ranging from Au-Au to p-p. It covers over five units of pseudorapidity, centered at η = 0, and covers full azimuth. Over one-third of its azimuth, it has two radial layers which allow it to determine the event vertex in three spatial dimensions. It is the primary detector in PHENIX for global event characterization and provides the fast LVL-1 multiplicity trigger to the entire PHENIX front end electronics.

The detector is comprised of a central barrel of silicon detector in multi-strip format and two 2π end-caps of silicon detectors arranged in pad format. The barrel is six-sided, centered about Z = 0 in PHENIX. The lowest two azimuthal sectors have two radial layers to enable event vertex finding. Over 34,000 channels of detector must be read out using electronics conforming to the standard PHENIX pipelined architecture and respecting the $\sim$5 mW/channel and compact space requirements of the MVD.

The general electronic processing chain includes a charge-sensitive preamplifier and discriminator, an analog memory unit allowing for LVL-1 trigger formation times of up to 4 μsec and as well as pipelined operation, a Wilkinson-type ADC, a current-mode summer for determining local particle multiplicity, and pipelined control logic. Specialized power and control cabling, motherboards to handle the several thousand signal lines, and interface modules to adapt MVD-internal signals to PHENIX transmission standards are also needed.

The preamplifier/discriminator is implemented as a 32-channel ASIC fabricated in HP's 1.2-micron N-well CMOS process. The charge sensitivity is 20 mV/fC, corresponding to 80-mV signals for minimum-ionizing particles incident normally to the silicon-strips. The discriminator is sensitive to 0.1 MIP and includes active reset circuitry to be active for all beam-crossings, which occur every 100 nsec. The discriminator outputs are summed in current mode for all 32 channels per ASIC to give an initial trigger output. An on-chip maskable pulser is included; serial string setup gives remote control over parameters.

The pulse-height output of TGV32 is sampled at 10 MHz in the AMUADC32, which is another 32-channel ASIC implemented in the same HP process. The analog memory section is 64 cells deep, partitioned to allow at least 40 cells for writing current events and at least 10 cells for holding two samples per triggered event for up to 5 triggered events. The ADC is a ramp-type operated with a 40-MHz two-edged clock and set for 10 bits operation. Fully pipelined operation has been demonstrated.

The control logic at the detector is implemented in a pair of Xilinx Field- Programmable Gate Arrays (FPGAs). One handles AMU list operations, and the other handles state machine functions and LVL-1 accept functions, as well as the serial-string downloads used to configure the TGV32 and AMUADC32.

The limited space available led to the decision to mount the electronics using High Density Interconnect technology on Multi-Chip Modules prepared by Lockheed Martin. This, in turn, required testing all ASICS using a wafer-probing technique before sawing to ensure better than 99.9% of chips used are good. FPGAs and an op-amp needed for the overall trigger summing were also selected to be known good die. Each MCM handles 256 channels of silicon detector and thus mounts 20 silicon die of electronics circuitry.

Interface cabling and motherboards (made by LANL) were prepared to connect the MCMs to Interface Modules (IMs) manufactured in VME-P form factor. These modules connect the MVD electronics to PHENIX standard timing, control, trigger, and readout modules. The Timing and Control IM receives clock and control data at 10 MHz via fiber optic from central control and passes copies to all MCMs and other IMs. The Data Collection IM receives ADC output data from MCMs and transmits it to Data Collection Modules in the control room. The Trigger IM receives fast trigger signals from the MCMs, flash encodes them to 8 bits, and transmits them at 40 MHz to LVL-1 logic in the control room. The ARCnet IM receives slow control data and prepares it for transmission to the MCMs. A last IM, TC34, was built to enable self-testing of the entire system prior to connection to the PHENIX DAQ.

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